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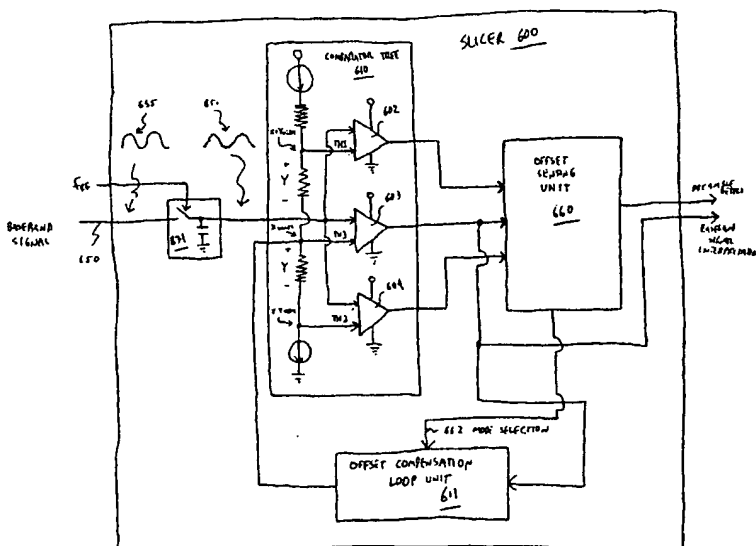
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(54) Title: **METHOD AND APPARATUS FOR COMPARATOR TREE STRUCTURE FOR FAST ACQUISITION OF OFFSETS  
INDUCED IN A WIRELESS RECEIVER**



(57) Abstract: A method that involves comparing an input signal (650) against a first threshold (TH1) and a second threshold (TH2) to generate a first thresholded signal and a second thresholded signal. The first threshold (TH1) is greater than the second (TH2) threshold. Then, detecting if the input signal (650) is above the first threshold (TH1) or below the second threshold (TH2) by comparing the first and second thresholded signals.



*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

## **Method and Apparatus For Comparator Tree Structure For Fast Acquisition of Offsets Induced In A Wireless Receiver**

The present application hereby claims the benefit of the filing date of a related Provisional Application filed on September 27, 1999, and assigned Application Serial No. 60/156,228.

### **FIELD OF THE INVENTION**

The field of invention relates to wireless receivers generally; and more specifically to a comparator tree structure that allows a receiver to quickly adjust to an offset in a baseband signal.

### **BACKGROUND**

#### Super Heterodyne and Frequency Shift Keyed (FSK) Modulation/Demodulation

Figure 1 shows a portion 106 of a receiving device 166 referred to as a demodulator. A demodulator 106 provides a signal (commonly referred to as a baseband signal  $b(t)$  in various applications) that is representative of the information being sent from a transmitting device 165 to a receiving device 166. The demodulator 106 extracts (i.e., demodulates) the baseband signal  $b(t)$  from a high frequency wireless signal that "carries" the baseband signal  $b(t)$  through the medium (e.g., airspace) separating the transmitting and receiving devices 165, 166.

The particular demodulator 106 example of Figure 1 is designed according to: 1) a demodulation approach that is commonly referred to as super heterodyne detection (hereinafter referred to as a heterodyne detection for simplicity); and 3) a modulation/demodulation scheme referred to as Frequency Shift Keying (FSK). The industry standard referred to as "BLUETOOTH" (the requirements of which may be found in "Specification of the Bluetooth System", Core v.1.0B, 12/1/99, and published by the Bluetooth Special Interest Group (SIG)) can apply to both of these approaches and, accordingly, will be used below as a basis for reviewing the following background material.

Heterodyne detection is normally used when dedicated channels are allocated within a range of frequencies 111 (where a range of frequencies may also be referred to as a "band" 111). For BLUETOOTH applications within the United

States, 89 channels  $110_1, 110_2, 110_3, \dots, 110_{79}$  are carried within a 2.400 GHz to 2.482 GHz band 111. Each of the 79 channels are approximately 1 Mhz wide and are centered at frequencies 1 Mhz apart.

The first channel  $110_1$  is centered at 2.402 Ghz, the second channel  $110_2$  is centered at 2.403 Ghz, the third channel  $110_3$  is centered at 2.404 Ghz, etc., and the seventy ninth channel  $110_{79}$  is centered at 2.480 Ghz. The heterodyne demodulator 106 accurately receives a single channel while providing good suppression of the other channels present within the band 111. For example, if channel  $110_2$  is the channel to be received, the baseband signal  $b(t)$  within channel  $110_2$  will be presented while the baseband signals carried by channels  $110_1$  and  $110_3$  through  $110_{79}$  will be suppressed.

An FSK modulation/demodulation approach is commonly used to transmit digital data over a wireless system. An example of an FSK modulation approach is shown in Figure 1. A transmitting modulator 105 within a transmitting device 165 modulates a baseband signal at a carrier frequency  $f_{\text{carrier}}$  into an antennae 102. That is (referring to the frequency domain representation 150 of the signal launched into the antennae 102) if the baseband signal corresponds to a first logic value (e.g., "1"), the signal 150 has a frequency of  $f_{\text{carrier}} + f_o$ . If the data to be transmitted corresponds to a second logic value (e.g., "0"), the signal has a frequency of  $f_{\text{carrier}} - f_o$ .

Thus, the signal launched into the antennae 102 alternates between frequencies of  $f_{\text{carrier}} + f_o$  and  $f_{\text{carrier}} - f_o$  depending on the value of the data being transmitted. Note that in actual practice the transmitted signal 150 may have a profile 151 that is distributed over a range of frequencies in order to prevent large, instantaneous changes in frequency. The carrier frequency  $f_{\text{carrier}}$  corresponds to the particular wireless channel that the digital information is being transmitted within. For example, within the BLUETOOTH wireless system,  $f_{\text{carrier}}$  corresponds to 2.402 Ghz for the first channel  $110_1$ . The difference between the carrier frequency and the frequency used to represent a logical value is referred to as the deviation frequency  $f_o$ .

Referring now to the heterodyne demodulator 106, note that the signal received by antennae 103, may contain not only every channel within the frequency band of interest 111, but also extraneous signals (e.g., AM and FM radio stations, TV stations, etc.) outside the frequency band 111. The extraneous signals are filtered by filter 113 such that only the frequency band of interest 111 is passed. The filter 113 output signal is then amplified by an amplifier 114.

The amplified signal is directed to a first mixer 116 and a second mixer 117. A pair of downconversion signals  $d1(t)$ ,  $d2(t)$  that are  $90^\circ$  out of phase with respect to each other are generated. A first downconversion signal  $d1(t)$  is directed to the first mixer 116 and a second downconversion signal  $d2(t)$  is directed to the second mixer 117. Each mixer multiplies its pair of input signals to produce a mixer output signal. Note that the transmitting modulator 105 may also have dual out of phase signals that are not shown in Figure 1 for simplicity. Transmitting a pair of signals that are  $90^\circ$  out of phase with respect to one another conserves airborne frequency space by a technique referred to in the art as single sideband transmission.

The frequency  $f_{\text{down}}$  of both downconversion signals  $d1(t)$ ,  $d2(t)$  is designed to be  $f_{\text{carrier}} - f_{\text{IF}}$ . The difference between the downconversion frequency  $f_{\text{down}}$  and the carrier frequency  $f_{\text{carrier}}$  is referred to as the intermediate frequency  $f_{\text{IF}}$ . Because it is easier to design filters 118a,b and 127a,b that operate around the intermediate frequency, designing the downconversion that occurs at mixers 116, 117 to have an output term at the intermediate frequency  $f_{\text{IF}}$  enhances channel isolation.

The mixer 117 output signal may be approximately expressed as

$$kb_{\text{FSK}}(t)\cos(2\pi f_{\text{carrier}} t)\cos(2\pi f_{\text{down}} t). \quad \text{Eqn. 1}$$

Note that Equation 1 is equal to

$$kb_{\text{FSK}}(t)[\cos(2\pi (f_{\text{carrier}} - f_{\text{down}})t) + \cos(2\pi (f_{\text{carrier}} + f_{\text{down}})t)] \quad \text{Eqn. 2}$$

which is also equal to

$$kb_{\text{FSK}}(t)\cos(2\pi f_{\text{IF}} t) + kb_{\text{FSK}}(t)\cos(2\pi (f_{\text{carrier}} + f_{\text{down}})t) \quad \text{Eqn. 3}$$

using known mathematical relationships. The  $b_{\text{FSK}}(t)$  term represents a frequency shift keyed form of the baseband signal (e.g., a signal that alternates in frequency between  $+f_0$  for a logical "1" and  $-f_0$  for a logical "0"). The constant  $k$  is related to

the signal strength of the received signal and the amplification of amplifier 114. For approximately equal transmission powers, signals received from a nearby transmitting device are apt to have a large  $k$  value while signals received from a distant transmitting device are apt to have a small  $k$  value.

Equation 3 may be viewed as having two terms: a lower frequency term expressed by  $kb_{FSK}(t)\cos(2\pi f_{IF}t)$  and a higher frequency term expressed by  $kb_{FSK}(t)\cos(2\pi (f_{carrier}+f_{down})t)$ . Filter 118b filters away the high frequency term leaving the lower frequency term  $kb_{FSK}(t)\cos(2\pi f_{IF}t)$  to be presented at input 119 of amplification stage 125. Note that, in an analogous fashion, a signal  $kb_{FSK}(t)\sin(2\pi f_{IF}t)$  is presented at the input 126 of amplification stage 170.

Amplification stage 125 has sufficient amplification to clip the mixer 117 output signal. Filter 127b filters away higher frequency harmonics from the clipping performed by amplification stage 125. Thus, amplification stage 125 and filter 127b act to produce a sinusoidal-like waveform having approximately uniform amplitude for any received signal regardless of the distance (e.g.,  $k$  factor) between the transmitting device and the receiving device.

After filter 127, a signal  $s(t)$  corresponding to  $Ab_{FSK}(t)\cos(2\pi f_{IF}t)$  is presented to the frequency to voltage converter 128 input 129 (where  $A$  reflects the uniform amplitude discussed above). The spectral content  $S(f)$  of the signal  $s(t)$  at the frequency to voltage converter 128 input 129 is shown at Figure 1. The signal  $s(t)$  alternates between a frequency of  $f_{IF} + f_o$  (for a logical value of "1") and a frequency of  $f_{IF} - f_o$  (for a logical value of "0"). The spectral content  $S(f)$  of the signal  $s(t)$  at the frequency to voltage converter 128 input 129 is mapped against the transfer function 160 of the frequency to voltage converter 128 in order to reproduce the baseband signal  $b(t)$  at the demodulator output.

### Frequency Synthesis

Referring back to the pair of downconversion signals  $d1(t)$ ,  $d2(t)$  that are directed to mixers 116, 117, recall that the downconversion signals  $d1(t)$  and  $d2(t)$  should have a downconversion frequency  $f_{down}$  equal to  $f_{carrier} - f_{IF}$  for each of the channels 110, through 110<sub>n</sub>. For example, for an intermediate frequency  $f_{IF}$  of

3Mhz, the frequency synthesizer 140 is responsible for generating a frequency of 2.399 Ghz in order to receive the first channel 110<sub>1</sub> (i.e.,  $f_{\text{carrier}} - f_{\text{IF}} = 2.402 - 0.003 \text{ Ghz} = 2.399 \text{ Ghz}$ ); a frequency of 2.400 Ghz in order to receive the second channel 110<sub>2</sub>; a frequency of 2.401 Ghz in order to receive the third channel 110<sub>3</sub>; . . . etc., and a frequency of 2.477 Ghz in order to receive the 79<sup>th</sup> channel 110<sub>79</sub>. A channel select input 141 presents an indication of the desired channel to the frequency synthesizer 140.

Both the transmitting device 165 and the receiving device 166 typically have a frequency synthesizer. A frequency synthesizer 140 is shown in the receiving device 166 (but not the transmitting device 165 for simplicity). Frequency synthesizers typically create their output signals by multiplying a reference frequency (such as the frequency of a local oscillator). As seen in Figure 1, frequency synthesizer 140 multiplies the frequency of local oscillator 142 to produce downconversion signals d1(t) and d2(t). For example, for a local oscillator 142 reference frequency of 13.000 MHz, frequency synthesizer 140 should have a multiplication factor of 184.53846 to produce downconversion signals d1(t), d2(t) used to receive the first channel 110<sub>1</sub> (i.e.,  $184.53846 \times 13.000 \text{ MHz} = 2.399 \text{ GHz}$ ).

A problem with wireless technology involves deviation from the "designed for" carrier  $f_{\text{carrier}}$  and/or downconversion  $f_{\text{down}}$  frequencies (e.g., from non zero tolerances associated with the local oscillator 140 reference frequency). As either (or both) of the carrier and/or downconversion frequencies deviate from their "designed for" values, offsets may be observed in the baseband signal b(t) at the demodulator 106 output.

Figure 2a shows a baseband signal 250 if the carrier and downconverting frequencies are ideal. As discussed above, the spectral content 253 of the signals produced by filters 127a,b will be centered at the intermediate frequency  $f_{\text{IF}}$ . Since the origin 250 of the frequency to voltage converter transfer curve 260 is centered at the intermediate frequency  $f_{\text{IF}}$ , the output signal 250 has no offset (e.g., has an offset positioned at 0.0volts)

Errors in the carrier and/or downconversion frequency, however, will cause the spectral content of the signals produced by filters 127a,b to be centered at an offset 254 from the intermediate frequency  $f_{if}$ . That is, because  $f_{if}$  in equation 3 corresponds to  $f_{carrier} - f_{down}$ , if either  $f_{carrier}$  or  $f_{down}$  (or both) are in error the value of  $f_{if}$  in equation 3 does not correspond to the designed for  $f_{if}$  value (e.g., 3Mhz) that is centered at the origin of the transfer curve 260. As such, the baseband signal 255 will have an offset 256 with respect to 0.0volts.

## SUMMARY OF INVENTION

A method that comprises comparing an input signal against a first threshold and a second threshold to generate a first thresholded signal and a second thresholded signal. The first threshold is greater than the second threshold. Then, detecting if the input signal is above the first threshold or below the second threshold by comparing the first and second thresholded signals.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the Figures of the accompanying drawings in which:

Figure 1 shows an embodiment of a demodulator;

Figure 2a shows a baseband signal without an offset;

Figure 2b shows a baseband signal with an offset;

Figure 3a shows a proper baseband signal interpretation;

Figure 3b shows an improper baseband signal interpretation;

Figure 4 shows an embodiment of a comparator having its threshold determined through a feedback loop;

Figure 5 shows an exemplary portion of a packet as received from a demodulator;

Figure 6 shows an embodiment of a slicer that can adjust its threshold to the offset of the signal shown in Figure 5;

Figure 7 shows exemplary signaling associated with the slicer embodiment of Figure 6;

Figure 8 shows a methodology executed by the slicer embodiment of Figure 6;

Figure 9 shows an exemplary embodiment of the offset sensing unit of Figure 6; Figure 10 shows an exemplary embodiment of a sample delay unit; and Figure 11 shows an exemplary embodiment of the offset compensation loop unit of the slicer shown in Figure 6.

#### DETAILED DESCRIPTION

A method is described that involves comparing an input signal against a first threshold and a second threshold to generate a first thresholded signal and a second thresholded signal. The first threshold is greater than the second threshold. Then, detecting if the input signal is above the first threshold or below the second threshold by comparing the first and second thresholded signals.

Another method is described that involves adjusting a first, second and third thresholds with a feedback loop. The feedback loop has a first bandwidth if a signal is above the first threshold or below the second threshold. The third threshold is below the first threshold and above the second threshold. The first, second and third thresholds are then adjusted by the feedback loop where the feedback loop has a second bandwidth if the signal is between the first and second thresholds. The first bandwidth is greater than the second bandwidth.

An apparatus is described of a first comparator having a first input that receives a first threshold and a second input that receives an input signal. The apparatus further comprises a second comparator having a first input that receives a second threshold where the second threshold is less than the first threshold. The second comparator also has a second input that receives the input signal. An offset sensing unit detects whether the input signal is above said first threshold or below said second threshold by comparing the first and second comparator outputs.

The method and apparatus described above, as well as other methods and apparatus, are discussed in more detail below.

Figure 3a shows a baseband signal 350 without an offset (similar to signal 250 of Figure 2b) while Figure 3b shows a baseband signal with an offset (similar to signal 255 of Figure 2b). As shown in Figure 3a, the determination as to whether or

not the baseband signal 350 corresponds to a logical 1 or a logical 0 depends upon the level of the baseband signal 350 with respect to a threshold 301a.

If the baseband signal 350 is above the threshold 301, the baseband signal is interpreted as a logical 1, if the baseband signal 350 is below the threshold 301, the baseband signal is interpreted as a 0. This activity may be referred to as thresholding, slicing, comparing and the like. Threshold level 301a shown in Figure 3 is properly positioned approximately midway between the positive and negative peaks 302a, 303a of the baseband signal 350. As a result, a correct digital interpretation 351 (e.g., having a 50% duty cycle) of the baseband signal 350 is formed as seen in Figure 3a. Note that the digital interpretation 353 of the baseband signal 350 is also commonly referred to as the baseband signal 353.

Referring to Figure 3b, if circuitry that performs the above described interpretation (typically referred to as a slicer or comparator) is unable to adjust (or unable to rapidly adjust) its threshold level 301b to an offset 356 in the baseband signal 355, the baseband signal 355 will be thresholded against an incorrect level (i.e., a level that is not approximately midway between the positive and negative peaks 302b, 303b of the baseband signal 355). An incorrect thresholding level 301b results in an incorrect digital interpretation 353 (e.g., excessive duty cycle distortion) as seen in Figure 3b.

For balanced coding schemes (i.e., schemes that transport data with an approximately equal number of 1s and 0s), such as those used within BLUETOOTH (as well as other wireless technology environments), the appropriate threshold level for a baseband signal may be determined by averaging the baseband signal. That is, referring to Figure 3b, the average value of the baseband signal (which is equal to its offset 356) is midway between the signal's positive and negative peaks 302b, 303b.

Figure 4 show a slicer embodiment 400 that is configured to automatically adjust its threshold level to the offset of the baseband signal by effectively averaging the slicer 400 output signal. The averaged demodulator 406 output signal is then applied as the threshold level of the slicer. The embodiment of

Figure 4 employs a comparator 410 that compares the baseband signal 450 at a first input 421 against a threshold at a second input 412. If the baseband signal 450 is greater than the threshold, the comparator 410 output is a logic "1". If the baseband signal is less than the threshold, the comparator 410 output is a logic "0".

Prior art receiving channels typically place an A/D converter and a slicer in series with one another after the demodulator output. That is, in prior art solutions, the baseband signal 450 is first converted from the analog domain to the digital domain by an A/D converter. The A/D converter produces a word of  $n$  bits (e.g., 6 bits) having a value representative of the baseband signal amplitude. The slicer then converts each A/D converter output word into a binary value (i.e., a "1" or "0") by comparing against a digital word that is representative of the threshold level.

Note that the approach of Figure 4 does not require an A/D converter between the demodulator 406 output and the slicer 400 input. That is, an analog comparator 410 may be used. The analog comparator 410 swings its output signal to the potential of either power rail (e.g., the supply node 470 potential for a logical "1" or the ground node 471 potential for a logical "0") depending upon the result of the comparison.

This approach may result in less expensive hardware costs because a binary interpretation of the baseband signal is obtained without the use of an A/D converter. In alternate embodiments, A/D conversion may be performed between the demodulator output and the comparator 410 input. As such, in these embodiments, the comparators 410 may be implemented as digital comparator.

For convenience, the term "baseband signal" and the like should be construed to cover either of these approaches. That is, the term "baseband signal" and the like should be construed as including an analog representation of the baseband signal or a digital representation of the baseband signal. Furthermore, the term "baseband signal" may be used to describe the input signal to a comparator regardless if the signal is the actual output of a demodulator 406 or the output some other functional block (such as a filter, A/D converter, etc.) that

processes the demodulator 406 output signal prior to the comparator. It is also important to point out that demodulator 406 may correspond to the demodulator design 106 of Figure 1 or another demodulator design different than the design shown in Figure 1.

In the slicer embodiment of Figure 4, a feed back scheme is used to control the comparator's threshold. The feed back loop 411 effectively averages the comparator 410 output signal in order to automatically adjust the comparator threshold level TH3 to the offset of the baseband signal 450. Details concerning possible embodiments of the feed back loop 411 are provided in more detail below.

A matter of concern is the speed at which the feedback loop 411 adjusts the slicer's threshold level. The term "loop bandwidth" may be used to refer to how quickly a feedback loop 411 can change a slicer's threshold level. A higher loop bandwidth corresponds to the ability to change the threshold level at a faster rate. Generally, during the initial moments of a received signal, more accurate comparator interpretations of the baseband signal 450 are achieved as the loop bandwidth increases.

Figure 5 demonstrates this property in more detail. Figure 5 shows a baseband signal 555. In Figure 5, a packet of information (hereinafter "a packet") sent by a transmitting device arrives at the receiving device at time T0. A corresponding offset 556 in the baseband signal 555 is observed (e.g., as caused by frequency synthesis inaccuracies that exist within the transmitting and/or receiving devices). Note that a grace period Tg may exist between the moment that a packet actually arrives T0 and the moment Tx that a change in offset is first observed.

This grace period Tg typically results from a latency designed into the transmitting device between the moment that the carrier frequency  $f_{\text{carrier}}$  begins to be transmitted and the moment the baseband signal (i.e., the packet) begins to be modulated (i.e., transmitted). Typically, in order to ensure that the entire packet is reliably sent, the transmission of the baseband signal is delayed by Tg after the carrier frequency  $f_{\text{carrier}}$  is enabled. It is important to point out, however, that the

teachings discussed herein are applicable to environments where no such latency exists (i.e., where  $T_g = 0$ ).

In order to accurately interpret the received packet, the slicer should rapidly adjust its threshold 501 to the baseband signal offset 556 by the time the grace period  $T_g$  expires. That is, referring back to Figure 4, the feedback loop 411 should have a sufficiently high bandwidth so that it can quickly respond to the change in offset.

By the nature of electronic circuits, however, the faster the loop is able to respond to an offset in the baseband signal (i.e., the higher the loop bandwidth), the more susceptible the slicer is to noise in the baseband signal during subsequent interpretations. That is, a slicer having high loop bandwidth tends to undesirably change its threshold in response to any noise spikes (e.g., noise spike 502) that appear on the baseband signal 555.

The change in threshold in response to a noise spike 502 can cause an incorrect interpretation 503 of the baseband signal 555 as seen in Figure 5. Slicers configured with a low loop 411 bandwidth have better immunity to noise. In a sense, because a low loop bandwidth is less capable of sudden threshold changes, the noise spike 502 exists for too brief a moment of time for the feedback loop (and therefore the threshold level) to respond to it.

An approach that enhances the overall interpretation of the baseband signal involves adjusting the feedback loop bandwidth in light of the difference between the offset 556 in the baseband signal and the slicer's threshold 501. Specifically, the loop bandwidth is increased as the difference between the threshold and the baseband signal offset increases.

Thus, if a large offset appears when a transmitting device begins to transmit to the receiving device, the slicer can rapidly adjust its threshold to the offset. **After the threshold is rapidly corrected for, the slicer "switches over" to a smaller loop bandwidth that provides sufficient noise immunity during subsequent interpretations of the baseband signal 555.**

This approach implies the presence of two functions. First, the ability to detect the proximity of the current thresholding level to the offset of the baseband signal. Second, the ability to calculate thresholds with different loop bandwidths in light of this detection. Both of these aspects are discussed immediately below.

Figure 6 shows a slicer embodiment 600 aimed at achieving the interpretation approach described just above. The slicer embodiment 600 includes a comparator tree 601, an offset sensing unit 660 and a feedback loop 611 that can operate at different loop bandwidths. The feedback loop 611 may also be referred to as an offset compensation loop 611 or offset compensation loop unit 611. The comparator tree 601 of Figure 6 provides a plurality of signals that may be analyzed in order to detect the proximity/remoteness of the slicer threshold to/from the baseband signal offset.

The comparator tree 601 has a plurality of comparators 602, 603, 604 that threshold (i.e., compare) a common input signal against different threshold levels. For example, as seen in the embodiment of Figure 6, three comparators 602, 603, 604 threshold a common input signal 651 against three different threshold levels a first threshold level TH1, a second threshold level TH2 and a third threshold level TH3. The thresholds may be established, as seen in Figure 6, by running a fixed current from a current source through a series of resistors. In an embodiment,

In various embodiments the threshold levels may be set equidistant from one another. For example, as seen in Figure 6, if the central threshold level TH3 corresponds to X volts, the upper TH1 and lower TH2 thresholding levels correspond to X+Y volts and X-Y volts respectively. As such, each threshold level is separated from its neighboring threshold level(s) by Y volts. In an embodiment, a resistor value of 1kohm and a current of 100 micro-amp are utilized to establish a threshold separation Y of 0.1 volts.

Embodiments employing an odd number of comparators (such as the exemplary embodiment of Figure 6) may use the centrally located threshold level (such as threshold level TH3 in Figure 6) as the "main" or "primary" threshold level. A main/primary threshold level is the threshold level against which the

baseband signal is actually interpreted. For example, if the interpretation provided by the comparator 603 is used to by circuitry downstream from the slicer.

The offset sensing unit 660 monitors the outputs of the comparator tree 601 to gauge the accuracy of the threshold. The offset sensing unit 660 provides the offset compensation loop 611 with a mode input 662 that controls the bandwidth of the offset compensation loop 611. In the embodiment of Figure 6, the mode provided by the offset sensing unit 660 is indicative of the difference between the primary slicer threshold level TH3 and the baseband signal offset.

For example, if the offset sensing unit 660 determines that the primary threshold TH3 is sufficiently inaccurate such that a rapid threshold adjustment is desired, the mode input 662 indicates to the offset compensation loop 611 that a high loop bandwidth should be used. Similarly, if the offset sensing unit 660 determines that the present threshold is sufficiently accurate, the mode input 662 indicates to the offset compensation loop 611, 612 that a lower loop bandwidth should be used.

The offset compensation loop 611 determines, according to the mode presented by the offset sensing unit 660, a threshold for the baseband signal and applies the threshold to the comparator tree 601. Note that in the embodiment of Figures 6a the offset compensation loop 611 applies the main threshold TH3 to a central comparator 602 and the outer thresholds TH1 and TH2 are formed by level shifting Y volts above and below the main threshold TH3.

It is important to note that, although the embodiment of Figure 6 only shows a comparator tree having three comparators 601, 602, 603, other embodiments may use a different number of comparators. Increasing the number of comparators generally increases the resolution at which the difference between a threshold and the baseband signal may be detected. Many designers may choose to use an odd number of comparators (e.g., 3, 5, 7, etc.) so that the centrally located comparator receives a primary threshold. Applying a primary threshold to a central comparator is not a strict requirement, however. Comparator trees having an even number of comparators are also possible.

Figure 7 shows signals associated with the slicer embodiment 600 of Figure 6. In Figure 7, similar to Figure 5, a packet arrives at time  $T_0$ . A grace period  $T_g$  exists between the moment that the packet arrives  $T_0$  and the moment a change in offset first occurs  $T_x$ . Referring to Figures 6 and 7, the comparator tree 601 embodiment of Figure 6 receives an analog baseband signal 655, 755 at its input 650.

The analog input signal 655, 755 is "chopped" by a sample and hold circuit 671 to form a sampled and held signal 651, 751. The sampled and held signal 651, 751 is presented to each of the comparators 602, 603, 604. The sampled and held signal 651, 751 allows the baseband signal 655, 755 to be easily converted into a stream a binary values as seen in more detail below.

The sampled and held signal 671, 751 may still be viewed as an analog signal, thus analog comparators 602, 603, 604 are used in the comparator tree 601 embodiment of Figure 6. The analog comparators 602, 603, 604 each perform a comparison of the sampled and held signal 651, 751 against their respective thresholds  $TH_1$ ,  $TH_3$  and  $TH_2$ . Figure 7 shows the threshold levels  $TH_1$ ,  $TH_3$ ,  $TH_2$  superimposed upon the sampled and held signal 751 for ease of understanding the comparator tree operation.

The slicer embodiment 600 of Figure 6 may be specially configured to capture or otherwise identify the arrival of a pre-determined pattern. For example, in BLUETOOTH applications, the first four symbols of a BLUETOOTH packet (referred to as its preamble 790) are a "1010" pattern 790 as seen in Figure 7. By identifying the arrival of the preamble 790 at time  $T_z$ , the receiving device gains an understanding as to where in time the packet's data 791 following the preamble begins. The receiving device can then re-align the phase of its internal clocks to properly time the reception and processing of the packet's information 791.

In order to recognize the reception of the preamble, the slicer embodiment 600 of Figure 6 may be designed with a number of different modes and corresponding offset compensation loop bandwidths. For example, in one embodiment the slicer 600 employs three different modes that are described in

more detail below. Note, however, that the slicer embodiment 600 of Figure 6 may be designed to have more or less than three modes. Furthermore, before continuing, it should be understood that the slicer embodiment of Figure 6 may be designed to support other mechanisms for reliable packet interpretation (e.g., including those that do not need to recognize a "1010" preamble, but rather, some other pre-determined data pattern).

A first mode, referred to as a "fast attack" mode, is used if the difference between the baseband signal offset 756b and the primary threshold level TH3 is too large for reliable interpretation of the baseband signal. The "fast attack" mode employs the highest offset compensation loop 611 bandwidth in order to quickly remove the large difference between the baseband signal offset and the threshold level TH3.

A second mode, referred to as the "preamble acquisition mode" is used if the difference between the baseband signal offset 756b and the primary threshold level TH3 is small enough to allow for reliable detection of the packet's preamble. Because the primary threshold level TH3 is deemed accurate during the preamble acquisition mode, the preamble acquisition mode offset compensation loop 611 bandwidth is less than the fast attack mode offset compensation loop 611 bandwidth.

A third mode, referred to as "tracking mode" is used after the preamble 790 has been detected. The tracking mode has the lowest offset compensation loop 611 bandwidth. The tracking mode is used to interpret the baseband signal 755 for the remainder of the packet following the preamble 790. As such, it is designed to have better noise immunity than the other modes. Note that the preamble acquisition mode may further refine the accuracy of the primary threshold TH3 such that, by the time the preamble is detected (i.e., when the acquisition is first entered), only slight adjustments (if any) are made to the primary threshold level TH3 by the tracking mode.

Figure 8 shows a methodology 800 for the transition from one slicer mode to another slicer mode. The methodology 800 of Figure 8 adjusts the slicer's loop

bandwidth in response to the accuracy of the present primary threshold level TH3 and the amount of accuracy and/or bandwidth needed for the particular state of a packet's reception. The following discussion of the methodology 800 of Figure 8 refers to the sampled and held baseband signal 751 and the primary threshold level TH3 shown in Figure 7.

Referring to Figures 6, 7 and 8, the preamble acquisition mode 801 may be viewed as the default mode of the slicer prior to the arrival of a packet. As such, before the baseband signal 755 offset changes (at time Tx) as a result of the transmitting device's carrier frequency being enabled, the slicer is "looking and waiting" for the arrival of the packet's preamble 790 in preamble acquisition mode 801. Before time Tx, in preamble acquisition mode 801, the slicer: 1) searches 810 for a comparator tree 601 output pattern that corresponds to the preamble 790 (via the offset sensing unit 660 as described in more detail below); 2) adjusts 811 its threshold TH3 toward the offset 756b of the baseband signal 755 (via the offset compensation loop 611); and 3) monitors 812 the accuracy of the primary threshold level TH3 by examining the comparator tree 601 output signals (via the offset sensing unit 660 as described in more detail below).

Just after time Tx, the baseband signal 755 offset changes to a new level 756b as a result of the transmitting device's carrier frequency being enabled. The offset sensing unit 660 detects 802 the inaccuracy of the primary threshold level TH3 (as described in more detail below) at time Ty1 and changes the mode of the offset compensation loop 611 to the fast attack mode 803.

The fast attack mode 803, as described above, employs a high loop bandwidth and therefore rapidly adjusts 820 the slicer threshold TH3. In this example, a fixed correction amount 725 is "force fed" to the threshold value TH3 that rapidly moves the threshold TH3 in the proper direction. As a result large, discrete adjustments are made to the threshold TH3 during fast attack mode as seen in Figure 7. Discrete adjustments are made to the threshold TH3 (i.e., the slicer remains in fast attack mode 803) until the threshold TH3 reaches an acceptable degree of accuracy (as determined by the offset sensing unit 660 as

described in more detail below) with respect to the offset level 756b of the baseband signal.

When the acceptable degree of accuracy is achieved, at time Ty2 in Figure 7, the offset sensing unit 660 triggers the slicer's re-entry to preamble acquisition mode 801. After the slicer returns to the preamble acquisition mode 801 after Ty2, the offset compensation loop 611 further improves the accuracy of the threshold TH3 as seen in Figure 7.

The slicer 600 remains in preamble detection mode 801 until the preamble 790 is detected by the offset sensing unit 660 (as described in more detail below) at time Tz. After the preamble is detected (i.e., after time Tz), the slicer enters tracking mode 804. The slicer output (i.e., from central comparator 602 in the embodiment of Figure 6) is presented to downstream circuitry so that information within the packet 741 following the preamble 790 can be processed. The offset sensing unit 660 can also provide the arrival of the packet (e.g., time T0 or time Tz as just two examples) to clock adjustment circuitry that adjusts the phase of the receiver's internal clocks.

Note that, because the preamble 790 is only four symbols wide (i.e., consumes a small amount of time), there is small likelihood that a noise spike will: 1) occur over the course of the preamble 790; and 2) have sufficient amplitude to disrupt the interpretation of the preamble 790. As such, the offset compensation loop 611 bandwidth used during preamble acquisition mode can afford to be greater than the offset compensation loop 611 bandwidth used during tracking mode.

Furthermore, the higher offset compensation loop 611 bandwidth associated with the preamble acquisition mode 801 (as compared to the tracking mode 804) provides the slicer 600 with enough bandwidth to quickly adjust for any inaccuracy in the threshold TH3 that remains after the rapid threshold adjustment performed by the fast attack mode 803. Thus, as described above, the slicer's offset compensation loop 611 bandwidth is reduced as the accuracy of the threshold TH3 improves.

Figure 7 shows the sampled and held signal 751 that is produced by the sample and hold circuit 671 of Figure 6. The sampled and held signal 751 is a common input signal that is presented to all three comparators 602, 603, 604 in the embodiment of Figure 6. The thresholds TH1, TH3 and TH2, as applied to the sampled and held signal, is also shown in Figure 7 superimposed upon the sampled and held signal 751.

The corresponding comparator output signals 702, 703, 704 are also shown in Figure 7. That is signal 702 corresponds to the output signal of comparator 602 which employs a threshold level of TH1, signal 703 corresponds to the output signal of comparator 603 which employs a threshold level of TH3, and signal 704 corresponds to the output signal of comparator 604 which employs a threshold level of TH2. These signals 702, 703, 704 help provide an understanding of the offset detection circuit 660 of Figure 6, a more detailed embodiment of which is shown in Figure 9.

In the offset sensing unit embodiment 960 of Figure 9, each comparator output is coupled to a sample delay unit 902, 903, 904. Thus, sample delay unit 902 is coupled to the output of comparator 602, sample delay unit 903 is coupled to the output of comparator 603 and sample delay unit 904 is coupled to the output of comparator 604.

Each sample delay unit 902, 903, 904 effectively queues samples from its corresponding comparator output signal. The number of comparator output samples stored in a sample delay unit 902, 903, 904 determines the size of a "sliding window" that effectively scans across the samples as they are taken from the comparator output. Figure 7 shows exemplary samples 705, 706, 707 taken from their corresponding comparator output signals. That is, sampling 705 is a series of samples taken from the first comparator 602 output signal 702, sampling 706 is a series of samples taken from the second comparator 603 output signal 703, and sampling 707 is a series of samples taken from the third comparator 604 output signal 704.

Samples are accumulated by effectively taking periodic "snapshots" of the comparator output signal value. For example, in the embodiment of Figure 7, the samples are taken at the same frequency  $f_{RF}$  that the switch in the sample and hold circuit 671 is modulated at. Thus, as seen in region 780 of sample stream 780 of Figure 7, the timing of each sample is aligned with the "held regions" of the sampled and held signal 751. That is, each comparator output signal sample is taken when the sample and hold circuit 671 holds the baseband signal 755.

Samples may be collected, for example, by clocking the value of the comparator output signal 702, 703, 704 into its corresponding sample delay unit 902, 903, 904. If the baseband signal symbol rate is known (e.g., 1.00 Mbit/s as in the case of BLUETOOTH), the frequency  $f_{RF}$  used to sample and hold the baseband signal and/or clock the comparator output samples into a sample delay unit may be a multiple of this rate (e.g., for 8:1 oversampling, an 8MHz frequency may be used).

Figure 10 shows an example of the sample delay unit 904 of Figure 9 embodied as a shift register 1004. A comparator output signal 704 value is clocked into the shift register 1004 input with each rising clock edge. Thus, each bit in the register corresponds to a comparator output signal sample. With each new rising clock edge, a new sample is taken (i.e., entered into the shift register in location 1) and the previous samples (i.e., the samples already existing in the shift register) move to the left one space. The leftmost sample (in location N) expires because it is over written by the sample value on its right. Collecting the samples in this manner corresponds to forming a sliding window that captures the most recent N samples of the comparator output signal (where N is the size of the register).

For example, as seen in Figure 7, at time  $T_p$  the preamble's first symbol 757 has fully arrived and the preamble's second symbol 758 is currently emerging. The contents of the shift register at time  $T_p$  correspond to the contents of window 782 seen in the lower comparator output sample stream 707. The window 782 effectively moves to the right after time  $T_p$  as new samples are entered into the

register 1004 input (on the right as seen in Figure 10) and the oldest, leftmost sample is expired.

Referring back to Figure 9, it is important to note that a sample delay unit 902, 903, 904 may be formed with approaches other than a shift register. For example, a first in first out (FIFO) queue may be used that builds up the state of the queue to N samples before removing the oldest sample from the queue. After building up the queue state to N samples, the oldest sample is serviced from the queue as each new sample is added. This keeps the queue state at N samples. Samples shift closer to the exit of the queue with each newly added sample.

As another embodiment, samples may be stored in a memory (e.g., a DRAM or SRAM chip external to the semiconductor chip having the slicer or embedded DRAM or SRAM space on the semiconductor chip having the slicer). The memory may be used to support other functions in the receiving device such as digital signal processor (DSP), microprocessor or filter. Rather than shifting older samples with each new sample, the circuitry used to control the memory addressing can be configured to rotate with modulo N such that the oldest sample in memory is continually overwritten.

Referring to Figures 6, 8 and 9, in light of the discussion of the slicer's operation provided above with respect to Figure 8, recall that the offset sensing unit 660, 960: 1) determines the mode used by the offset compensation loop 611 in light of the accuracy of the threshold level (and/or the occurrence of a significant event such as the recognition of a packet's preamble); and 2) analyzes the comparator tree 601 output samples 705, 706, 707 in search of the packet's preamble 790. Both of these operations are discussed immediately below.

Referring to the offset sensing unit 960 of Figure 9, note the presence of correlation units 912, 913, 914 respectively coupled to each sample delay unit 902, 903, 904. A correlation is a mathematical technique that may be used to compare the similarity of two data patterns. To perform a correlation, typically, a first data pattern is convoluted with a second data pattern.

The result of the correlation is a "spike", the height of which provides a measurement of the degree of similarity between the two data patterns. That is, the more similar the pair of correlated data patterns (as to their shapes, features, etc.), the higher the height of the spike becomes. Thus, if a pair of identical data patterns are correlated, the spike resulting from their convolution has a maximum height. If the pair of completely dissimilar data patterns are correlated, the spike has no height (i.e., does not exist). More information regarding correlation may be found in a U.S. Patent entitled Method and Apparatus for Identifying a Pre-Determined Pattern from a Received Signal Via Correlation filed on September 27, 2000.

The collection of samples in each sample delay unit 902, 903, 904 may be viewed as a data pattern. Each of these data patterns are correlated with a previously stored data pattern by their respective correlation unit. Thus, the data pattern held in sample delay unit 902 is correlated against a previously stored data pattern by correlation unit 912, the data pattern held in sample delay unit 903 is correlated against a previously stored data pattern by correlation unit 913, the data pattern held in sample delay unit 904 is correlated against a previously stored data pattern by correlation unit 914.

The previously stored data patterns may be supplied (directly or indirectly) by a read only memory 921 (ROM) and stored in registers 915, 916, 917 that are respectively coupled to a correlation unit 912, 913, 914 (as shown in Figure 9). Registers 915, 916, 917 allow for quick access of the previously stored data patterns by the correlation units 912, 913, 914.

The slicer effectively "looks for" particular comparator output sample stream patterns by correlating the previously stored data patterns with the contents of the sample delay units 902, 903, 904. In an embodiment, correlations are performed for each position of the sliding window (i.e., separate correlations are performed after each new comparator output sample). Thus, each correlation unit 912, 913, 914 continually "checks" the most recent collection of comparator output samples to see if they "match" a predetermined "looked for" pattern.

In an embodiment, during preamble acquisition mode, the correlation units 902, 903, 904 continually correlate comparator output samples against a pre-determined data pattern in search of comparator output sample patterns that indicate either the need to place the slicer in fast attack mode or the fact that the preamble has arrived. This is achieved by correlating comparator output samples against a first pre determined data pattern (to understand if fast attack mode is needed) and a second pre determined data pattern (to understand if the preamble is arrived). Note that if the baseband signal has a small offset (i.e., within TH1 and TH2), the fast attack mode is simply not entered.

Note that registers 915, 916, 917, as drawn in Figure 9, should have space available for both patterns. That is, for example, register 915 is partitioned into two sections 918, 919. Section 918 may be used to store the first pattern while section 919 may be used to store the second pattern. Registers 916 and 917 are similarly partitioned into spaces 920, 921 and 922, 923.

Referring to region 783 of the comparator samples 705, 706, 707 in Figure 7 (i.e., just after the baseband signal changes its offset at time Tx), note that the values of the samples are equal in value once the sampled and held signal 751 falls below the lower threshold TH2. That is, just after time Tx, the sampled and held signal 751 falls below all three thresholds TH1, TH3 and TH2. This causes each of the comparators 602, 603, 604 to produce an output value of "0" as seen in signals 702, 703, 704.

Entry into Fast Attack mode may be triggered upon comparing the output signals 702, 703, 704 or samples 705, 706, 707. Specifically, if signals 702 and 704 or samples 705 and 707 are equal, the offset 556b is outside TH1 and TH2. These comparisons may be enhanced by the use of correlation techniques as discussed in the embodiments that follow.

If the correlation units 912, 913, 914, continually correlate the contents of the sample delay units 902, 903, 904 with a previously stored data pattern (located in registers, 915, 916, 917) that correspond to a string of 0s (e.g., 00000000), the height of the correlation "spike" produced at the Fast\_Attack\_Down correlation unit

outputs 967, 968, 969 becomes larger as the samples of region 783 begin to accumulate in the sample delay units 902, 903, 904. The correlation units 912, 913, 914 may be designed to trigger a "match", signifying the looked for data pattern has been found, when the correlation "spike" reaches or surpasses a specific height. The specific height may vary from embodiment to embodiment depending on the density of samples, the size of the grace period  $T_g$ , etc.

As an example, assume that a previously stored eight bit pattern, 00000000, is correlated by each correlation unit 912, 913, 914 against the contents of its corresponding sample delay unit 902, 903, 904. The height of the FAST ATTACK correlation spikes from each correlation unit 912, 913, 914 will be a maximum at time  $T_{y1}$  of Figure 7 because, as of time  $T_{y1}$ , eight consecutive 0s will be located in each 902, 903, 904 sample delay unit.

If the threshold for triggering a match is the maximum spike height (e.g.,  $X$  as thresholded by comparison units 910a,b,c), all three correlation units will simultaneously trigger a match after the correlation performed at time  $T_{y1}$  in Figure 7. When each Fast\_Attack\_Down output 967, 968, 969 simultaneously indicates a match at time  $T_{y1}$ , a fast attack mode bit 749 is set, which (referring briefly to Figure 6) is communicated to the offset compensation loop 611. This activity acts as a comparison of the sample stream values 705, 706, 707.

As the baseband signal 751 rises above the lower threshold level TH2 after time  $T_{y1}$ , the correlation spike from the lower correlation unit 914 will begin to fall because logic 1s begin to enter its sample and hold unit 904. The falling correlation spike causes the Fast\_Attack\_Down output 969 to drop which consequently drops the FA\_DOWN bit 749 from the AND gate 977. This causes the slicer's offset compensation loop to re-enter the preamble acquisition mode as discussed with respect to Figure 8.

Before continuing with a discussion of the correlation used to detect the preamble, a few points are worth mentioning regarding the entry/de-entry to/from fast attack mode discussed just above. First, note that if the baseband signal 755 were to have an offset polarity opposite that shown in Figure 7 (i.e.,

such that the baseband signal rises above the TH1 threshold rather than below the TH2 threshold level), region 783 would comprise "1"s rather than "0s".

Thus, the first data pattern described above used to detect whether or not fast attack mode is needed may actually be implemented with two data patterns: one being a consecutive string of 0s (to detect demodulator signals below TH2) and one being a consecutive string of 1s (to detect demodulator signals above TH1). These may be correlated in series or in parallel with one another.

Consistent with this approach, note that two "fast attack" outputs are utilized. The first Fast\_Attack\_Down outputs 967, 968, 969, as discussed above, signify that the baseband signal is below all three threshold levels TH1, TH3, TH2. The set of Fast\_Attack\_Up outputs (which correlate against a string of consecutive 1s) signify that the baseband signal is above all three threshold levels TH1, TH3, TH2. As a result two fast attack mode bits are formed at the output of the offset sensing unit 960: FA\_UP and FA\_DOWN. If the FA\_UP bit is high, the threshold levels will be moved up by the offset compensation loop. If the FA\_DOWN bit is high the threshold levels will be moved down by the offset compensation loop.

Furthermore, if the demodulator exhibits less than perfect channel isolation, it is possible that the low power (i.e., small amplitude) baseband signals from channels other than the channel to be received will be presented to the slicer. Signals may be deemed "qualified" for further processing if they have an amplitude outside the outer thresholds (i.e., above TH1 and below TH3). This acts akin to a signal detect that ignores the weaker, low amplitude signals from an incorrect channel.

Also, note that based on the spacing Y between the threshold levels (in light of the amplitude of the preamble signal), temporal regions 784, 785, 786 and 787 of simultaneously equal comparator output signal samples appear near/at the peaks 788, 789, 790, 791 of the preamble. Note however, these regions have a smaller width W2 than the width W1 of the region 783 that triggered the fast attack mode.

If W1 and W2 were equal in width, the slicer could mistakenly "misidentify" the peaks 788, 789, 790, 791 of the preamble as a need for entry to the

fast attack mode. That is, the "fast attack match" outputs 967, 968, 969 would simultaneously indicate a match (setting the fast attack mode bit high) for each peak 788, 789, 790, 791 of the preamble because the same number of consecutive, equal logic values would exist in region 783 as in regions 784, 785, 786 and 787.

However, as W1 is made greater than W2 (i.e., as more consecutive, equal logic values are looked for in order to trigger the fast attack mode), the height of the correlation spikes produced in regions 784, 785, 786, 787 fall below the height of the spike produced by the correlations in region 783. That is, as less consecutive, equal values exist in regions 784, 785, 786, 787 they do not significantly resemble the looked for pattern. Better said, the looked for pattern in the example of Figure 7 has eight consecutive equal values while the preamble is only capable of producing five.

The difference in correlation spike height as between region 783 and regions 784, 785, 786, 787 may be used to prevent the slicer's entry into fast attack mode during the reception of the preamble. That is, the higher the spike height associated with region 783 is sufficient to set the "fast attack match" outputs 967, 968, 969 while the lower spike height associated with regions 784, 785, 786, 787 are not.

Note that the width W2 of regions 784, 785, 786, 787 may be controlled by designing for a certain preamble amplitude against specific TH1 and TH2 levels. That is, as the TH1 level moves closer to the maximum preamble peak and the TH2 level moves closer to the minimum preamble peak, the width W2 of regions 784, 785, 786 and 787 becomes smaller. At an extreme, they may be designed such that TH1 is above the maximum preamble peak and TH2 is below the maximum preamble peak.

In this case, W2 is zero (i.e., regions 784, 785, 786 and 787 do not exist). This allows for a minimal usable width W1 for region 783. That is, the correlation spike height used to "catch" the need for the fast attack mode may be minimal because no spike is produced at the preamble peaks. Note that a smaller region 783 width

W2 corresponds to the slicer's ability to identify the need for fast attack mode sooner. That is, time  $T_{y1}$  moves closer to time  $T_x$  as W2 shortens.

Workable ranges of W2 and W1 bring forth a tradeoff between the fast attack mode offset compensation loop bandwidth and the preamble acquisition mode offset compensation loop bandwidth. As W2 is reduced, the slicer can identify the need for the fast attack mode sooner (i.e.,  $T_{y1}$  is closer to time  $T_x$ ). This allows for a lower fast attack mode offset control loop bandwidth because for a given grace period  $T_g$ , the fast attack mode has more time to correct for the threshold error.

However, reducing W2 creates the need for an even smaller W1 (so that the fast attack mode is not inadvertently triggered during the arrival of the preamble). Reduced W1 may be produced by moving the threshold levels TH1, TH2 farther away from TH3 (i.e., increasing their spacing Y). Having increased threshold spacing Y means the slicer can re-enter preamble acquisition mode with a greater remaining threshold error.

That is, since the slicer re-enters the preamble acquisition mode when TH1 rises above the baseband signal falls or TH2 falls below the demodulator signal, this leaves a remaining threshold error approximately equal to Y for the offset compensation loop to correct for. In order to correct for the remaining threshold error (Y) before the preamble arrives, larger offset compensation loop bandwidths may be used during preamble acquisition mode for slicers designed with a large Y as compared to the offset compensation loop bandwidths that may be used during preamble acquisition mode for slicers designed with a small Y.

Note that as an alternative embodiment, rather than storing a predetermined fast attack mode pattern in a register (as described above) and correlating it against the comparator output signal samples, the contents of the sample delay units may be correlated with one another. When the samples are equal, as in region 783, a large correlation spike will be produced. Thus, rather than sending the contents of each sample delay line unit 902, 903, 904 to its own

correlation unit 912, 913, 914, they may alternatively be delivered to a single correlation unit capable of performing a correlation between three sets of samples.

Correlation units 902, 903, 904 may be formed by hardwired logic (such as within an application specific integrated circuit (ASIC) or standard product offering), programmable logic (as within an field programmable gate array (FPGA) or other programmable technology) or by a digital signal processor or microprocessor that executes software configured to execute the methodology described above.

Detection of the preamble may be made by methods similar to those described above. That is, a predetermined pattern of samples (that resemble the samples that should appear in the sample delay units when the preamble arrives) is stored in a register and correlated against the sample delay unit's samples. In an embodiment, the sample delay units are four symbols wide so that the entire preamble can be stored in the sample delay units when it arrives. Exemplary predetermined patterns 795, 796, 797 for this approach are shown in Figure 7 (using the sample streams 705, 706, 707 for simplicity) for each of the three correlation units 912, 913, 914 respectively.

Note that, by design, the predetermined patterns 795, 796, 797 match the received data samples of Figure 7. The height of the correlation spikes correlated against these patterns 795, 796, 797 will reach a maximum when the preamble is fully stored in the sample delay units 902, 903, 904. This will trigger a logic high at the "preamble detect" outputs 991, 992, 993 of the correlation units 912, 914, 913. Note that noise or other "bit flips", as well as some error in the threshold level should be accounted for when determining the acceptable correlation spike height for preamble detection.

For example, notice that the looked for sample pattern 786 from the central comparator sample stream 706 has a 50-50 duty cycle. In reality, the central threshold level TH3 may not be perfect when the preamble arrives - resulting in a duty cycle other than 50-50 in the samples collected by the central sample delay unit 902. The effect will be a lower correlation spike height for the preamble's

samples (as compared to a perfectly thresholded preamble). Thus, some margin for lower, acceptable spike heights may be designed into the correlation units 912, 913, 914.

Note that the predefined data patterns utilized by each correlation unit during their search for the preamble have different duty cycles because of the different thresholds used by each comparator. Those of ordinary skill will be able to determine the appropriate oversampling rates, correlation spike heights, etc. that are acceptable for a desired amount of threshold error, duty cycle distortion, etc.

Figure 11 shows an embodiment 1111 for the offset compensation loop 611 of Figure 6. Recall that the offset compensation loop 611 effectively averages the baseband signal 650 to produce a threshold against which the baseband signal may be sliced. Also recall that the offset compensation loop operates at different bandwidths depending on the appropriate slicer mode as determined by the offset sensing unit 660.

Specifically, the slicer embodiment of Figure 11 has three operative modes: 1) a fast attack mode; 2) a preamble acquisition mode; and 3) a tracking mode. Under the fast attack mode, the offset compensation loop operates at its highest bandwidth. Under the tracking mode, the offset compensation loop operates at its lowest bandwidth. Under the preamble acquisition mode, the offset compensation loop operates at a bandwidth between its highest and lowest bandwidths.

In the offset compensation loop embodiment of Figure 1111, the Fast Attack\_UP, Fast Attack\_DOWN and Preamble Detect input lines are the Fast Attack\_UP, Fast Attack\_DOWN and Preamble Detect output lines associated with the offset sensing unit 960 of Figure 9. Control chart 1101 of Figure 11 indicates how the input bits are used to control the mode of the offset compensation loop. Operational characteristics used by all the modes are discussed first, followed by a discussion of the operational characteristic unique to each mode.

The offset compensation loop embodiment of Figure 11 includes an accumulator 1104, a scaling unit 1105 and a digital to analog (D/A) converter 1106.

The offset compensation loop 1111 is designed from the perspective of an error term. In the embodiment of Figure 11, the error term is a digital word (i.e., a plurality of bits) that is presented to the input of the accumulator 1104.

The error term has two components: a polarity and a value. For a particular threshold adjustment, the polarity of the error term controls the direction of the adjustment (i.e., up or down) while the value of the error term controls the amount of the adjustment (i.e., how many volts the threshold is adjusted). Because a higher loop bandwidth corresponds to faster threshold adjustments (i.e., greater adjustment per unit of time) as compared to a lower loop bandwidth, the bandwidth of the offset compensation loop 1111 is controlled by controlling the magnitude of the error term value.

Thus, the fast attack mode employs large error term values so that large adjustments are made to the threshold per unit time. Similarly, the tracking mode employs small error term values so that small threshold adjustments are made per unit of time. The preamble acquisition mode employs error term magnitudes in between the large and small magnitudes associated with the other two modes so that medium adjustments are made to the threshold per unit of time.

A series of individual error terms are clocked sequentially into the accumulator 1103. The accumulator "accumulates" the individual error terms which, over time, add up to a value that corresponds to the proper adjustment. An accumulator 1103 may be formed as shown in Figure 11 with an adder 1108 having its output node coupled to a storage element 1109 (e.g., a register or flip-flop capable of holding the adder 1108 output word) where the storage element is coupled (via a feedback arrangement) to one of the accumulator input nodes 1110.

In order to produce a new accumulator output value (which corresponds to a new adjustment to be made to the threshold level), the accumulator 1103 adds its current output value to a new error term. That is (in the embodiment of Figure 11) when a new error term is presented to the adder 1108, the adder 1108 presents the storage element 1109 with the summation of the accumulator's current output value and the new error term. This summation is then clocked into the storage

element 1109 to produce a new accumulator output value. New accumulator output values can therefore be presented at the rate of the clock coupled to the storage element.

The accumulator output value may then be scaled again (at the designer's option) with a scaling unit 1104. The scaling unit 1105 multiplies the value of the accumulator output word by a constant. The output word of the scaling unit 1105 (if used) or the output word of the accumulator 1103 is then applied to a digital to analog converter 1106. The digital to analog converter 1106 converts the value of the digital word presented at its input into a corresponding DC voltage at its output. This voltage is then applied to the input of the comparator tree (at threshold level TH3) as shown back in Figure 6.

Recall from above that the error term controls the size and direction of a threshold adjustment. Error term unit 1112 is responsible for determining the error term. This error term unit 1112 may be viewed as being partitioned into two regions 1113, 1114. A first region 1113 determines the error term when the slicer is in fast attack mode. A second region 1114 determines the error term when the slicer is not in fast attack mode.

The output of the active region 1113, 1114 (i.e., region 1113 if the slicer is in fast attack mode or region 1114 if the slicer is not in fast attack mode) is presented to the accumulator by multiplexer 1115. The channel select input 1116 of the multiplexer 1115 is controlled, in the embodiment of Figure 11, by the state of the fast attack mode inputs 1116, 1117. If either of the fast attack mode inputs 1116, 1117 are a logic high (signifying the slicer is to be placed in fast attack mode), the multiplexer 1115 enables the output of region 1113.

Region 1113 (the fast attack region) creates an error term having a fixed value ("Z"). The polarity of the error term is based upon the direction the threshold needs to be adjusted. Presenting a negative value to the accumulator input will lower the accumulator output value (which consequently lowers the threshold). Similarly, presenting a positive value to the accumulator input will raise the accumulator output value (which consequently raises the threshold).

The channel select input 1120 of the multiplexer is configured to enable the proper polarity error term in light of the fast attack mode inputs. Thus, if the threshold needs to be lowered (as indicated by a logic low on the fast attack mode\_UP input 1117) an error term of  $-Z$  is forwarded to multiplexer 1115. Similarly, if the threshold needs to be raised (as indicated by a logic high on the fast attack mode\_UP input 1117) an error term of  $+Z$  is forwarded to multiplexer 1115.

Note that  $Z$  can be implemented as a digital word of  $n$  bits. In order to ensure that the fast attack mode has a higher bandwidth than the other modes, the value of  $Z$  may be configured to be equal to or greater than the maximum possible error term from region 1114 (although note that this is not an absolute requirement). Because the value of  $Z$  is fixed, the series of error terms produced by error term unit 1112, while the slicer is in fast attack mode, will also be fixed.

As a consequence, the adjustments made by the offset compensation loop to the threshold are the same. Recall this feature was originally shown and discussed in Figure 7. That is after time  $T_{y1}$  in Figure 7, when the slicer operates in fast attack mode, note the fixed series of adjustments made to the threshold. Applying a series of large, fixed error terms when in fast attack mode input allows the slicer to have a stable, high bandwidth offset compensation loop (i.e., the large overshoot and long settle time associated with higher bandwidth loops is avoided).

When the slicer is not in fast attack mode, it is either searching for the preamble with a moderate loop bandwidth or, having found the preamble, is actively tracking the baseband signal symbols that follow the preamble with a low loop bandwidth. Region 1114 determines the error term in either of these modes. The different loop bandwidths are controlled by adjusting the scaling of a subtractor 1122 output as discussed in more detail below.

The subtractor 1122 takes the difference between two values. The first value is 0.500. The second value is the average over a previous number of center comparator output samples. That is, a sample delay unit 1123 (similar to the sample delay unit 903 of Figure 9) collects the most recent number of center delay

samples (up to a certain amount) to effectively form a sliding window as discussed with respect to Figures 7 and 9.

The samples in the sample delay unit 1123 are averaged by averaging logic 1124. Note that the contents of the sample delay unit 1123 are binary (i.e., a "1" or a "0"). Thus the average produced by averaging unit 1123 ranges between a maximum of 1.000 (when the sample delay unit 1123 contains only 1s) and a minimum of 0.000 (when the sample delay unit 1124 contains only 0s). The average obtained by the averaging unit 1124 is then presented to the subtractor 1122.

The subtractor 1122 subtracts 0.500 from the output of the averaging unit 1124. The subtractor 1122 produces a preliminary error term (e.g., as just a few examples: -0.500 for an average of 0.000; -0.250 for an average of 0.250; 0.000 for an average of 0.500, 0.250 for an average of 0.750, and 0.500 for an average of 1.000) having a polarity and magnitude indicative of the adjustment that should be made to the present threshold level.

If the polarity of the subtractor 1122 output is negative, the output of the averaging unit 1124 is less than 0.500 (because more than half the samples are a logic 0) which indicates the current threshold level is above the average value of the baseband signal. In this case, the threshold should be lowered. Adding the negative subtractor output (or a scaled version of it) to the current accumulator value will properly lower the value of the current threshold level.

Similarly, if the polarity of the subtractor 1122 output is positive, the output of the averaging unit 1124 is greater than 0.500 (because more than half the samples are a logic 1) which indicates the current threshold level is below the average value of the baseband signal. In this case, the threshold should be raised. Adding the positive subtractor output (or a scaled version of it) to the current accumulator value will properly raise the value of the current threshold level.

A larger subtractor unit output magnitude indicates the threshold is farther away from the baseband signal average than a smaller subtractor unit output. That is, a threshold level that produces an averaging unit 1124 output value of + or

- 0.750 is farther away from the baseband signal offset than a threshold level that produces an average output value of + or - 0.250.

The magnitude of the change made to the accumulator output is related to the magnitude of the subtractor 1122 output. That is, a large subtractor 1122 output magnitude value produces a greater change to the accumulator output value (which consequently produces a larger threshold adjustment) than a small subtractor output magnitude. Thus, for example, a subtractor 1122 output value of 0.750 will produce a greater adjustment to the threshold than a subtractor 1122 output value of 0.250.

These principles of design are inherently stable. That is, the threshold level is raised/lowered as its position falls below/above the baseband signal average; and, furthermore, the amount the threshold is adjusted increases/decreases as the threshold becomes farther from/closer to the baseband signal average. As a natural result of this stability, the threshold continually approaches and eventually settles to a level that produces an averaging unit 1124 output of 0.500. Because an averaging unit 1124 output of 0.500 corresponds to the threshold being placed at the baseband signal offset, the threshold settles at the demodulator signal offset.

This is seen in Figure 7 during the slicer's preamble acquisition mode operation prior to time Tx (when the transmitting device's carrier arrives) and after time Ty2 when the slicer exits fast attack mode. Prior to time Tx, the slicer has already stabilized at the baseband signal average. As a result, the central comparator randomly "chatters" from the baseband signal noise. The random noise produces approximately equal numbers of 1s and 0s which corresponds to an average value of 0.500.

After time Ty2, the slicer re-enters the preamble acquisition mode. Referring to Figure 11, note that the entry of the slicer into fast attack mode causes the sample delay unit 1123 to "clear" (i.e., empty its contents). Thus, at time Ty2 when the slicer re-enters preamble acquisition mode, the sample delay unit 1123 begins to accumulate fresh central comparator samples.

Because the central threshold level TH3 is still above the baseband signal at time Ty2, the sample delay unit 1123 immediately begins to accumulate samples having a value of "0" which results in an average value of 0.000. This produces a negative term at the subtractor 1122 output which further lowers the central threshold TH3 as seen in Figure 7. The central threshold TH3 eventually settles to the baseband signal offset.

The preamble acquisition mode's loop bandwidth is a function of scaling unit 1125 and the depth of the sample delay unit 1123 (i.e., how many samples the scaling unit holds). Generally, the loop bandwidth increases as the scaling unit k1 increases and the sample delay unit 1123 depth decreases. Scaling unit 1125 effectively multiplies the preliminary output term from the subtractor 1122 by a constant k1.

Thus, for a given subtractor 1122 output value magnitude, a larger k1 presents a larger magnitude input to the accumulator (causing a larger adjustment to the threshold level) than a smaller k1. Similarly, a smaller sample delay unit 1123 depth allows the subtractor output to reflect sudden changes in the position of the baseband signal (with respect to the threshold level TH3) because each sample has a greater weight in the average that is calculated by the averaging unit 1124.

If the preamble has not been found, as discussed above, the slicer will be in preamble acquisition mode (unless it is in fast attack mode). The preamble detect input 1118 (provided by the offset compensation loop unit) indicates whether or not the preamble has been found and may therefore be used to control the loop bandwidth. As seen in Figure 11, if the preamble found input 1118 is low (indicating the preamble has not been found), the scaling unit 1125 has a scaling factor of k1. Alternatively (or in combination) a first sample delay unit 1123 depth may also be established.

After the preamble is found, the preamble detect input 1118 goes high and the slicer enters tracking mode. The scaling unit 1125 is adjusted to have a lower scaling k2 (where  $k_1 > k_2$ ) as a result. Because k2 is less than k1, the magnitude of

the error terms presented to the accumulator 1103 (for an identical subtractor 1122 output value) will be lower when the preamble is found. This corresponds to a lower loop bandwidth. Alternatively, or in combination, the depth of the sample delay unit 1123 may be increased as compared to the depth employed during the preamble acquisition mode.

Note that sample delay unit 1123 may be a separate sample delay unit from the sample delay unit 903 of Figure 9 (which also collects samples from the central comparator's output signal). Alternatively, sample delay unit 1123 used in the offset compensation loop 1111 may be the same sample delay unit 902 employed in the offset sensing unit. The front portion(s) of sample delay unit 902 may be used (rather than its entire contents) for sample delay unit 1123 if the depth of sample delay unit 1123 is to be less than the depth of sample delay unit 903.

As an alternative embodiment, the sample delay unit 1123 and averaging unit 1124 may be disposed of. That is, the samples from the center comparator may be fed directly into the subtractor 1122. This approach is also inherently stable. That is, the central threshold level TH3 will approach and eventually settle to the average of the baseband signal.

Referring to Figure 6, note that other offset sensing approaches may be configured to observe the output signals from a comparator tree arrangement and/or other offset compensation loop approaches may be configured to adjust the threshold level of a comparator tree arrangement, besides those discussed above. Once the pre-determined pattern (e.g., preamble) is discovered, the central comparator 602 output signal will provide a correct interpretation of the baseband signal (similar to that seen in Figure 3a). As such the center comparator 602 output signal may be forward to downstream circuitry as the slicer output.

It is important to point out that the discussion above is applicable to other applications besides preamble detection for a BLUETOOTH device. The teachings above may be applied to any receiver desiring to identify a particular data sequence (i.e., a predetermined pattern). That is, sequences other than a 1010

preamble (e.g., such as a synchronization word within a BLUETOOTH packet) may be found by techniques similar to those described above.

Furthermore, it is also important to note that the present teachings may be used to detect any predetermined pattern from a signal having a sudden offset. Thus, the present teachings are also applicable to other frequency shift keyed wireless technologies besides BLUETOOTH such, as just a few examples, HomeRF, IEEE 802.11, GSM and Digitally Enhanced Cordless Telephony (DECT).

Embodiments of the above discussion may be manufactured as part of a semiconductor chip (e.g., by a planar semiconductor manufacturing process). Note also that embodiments of the present description may be implemented not only as part of a semiconductor chip but also within machine readable media. For example, the designs discussed above may be stored upon and/or embedded within machine readable media associated with a design tool used for designing semiconductor devices. Examples include a netlist formatted in the VHSIC Hardware Description Language (VHDL) language, Verilog language or SPICE language. Some netlist examples include: a behavioral level netlist, a register transfer level (RTL) netlist, a gate level netlist and a transistor level netlist. Machine readable media also include media having layout information such as a GDS-II file. Furthermore, netlist files or other machine readable media for semiconductor chip design may be used in a simulation environment to perform the methods of the teachings described above.

Thus, it is also to be understood that embodiments of this invention may be used as or to support a software program executed upon some form of processing core (such as the CPU of a computer) or otherwise implemented or realized upon or within a machine readable medium. A machine readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical

or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

**CLAIMS**

What is claimed is:

1. An apparatus, comprising:
  - a) a first comparator having a first input that receives a first threshold and a second input that receives an input signal;
  - b) a second comparator having a first input that receives a second threshold, said second threshold less than said first threshold, said second comparator having a second input that receives said input signal; and
  - c) an offset sensing unit that detects said input signal above said first threshold or below said second threshold by comparing said first and second comparator outputs.
2. The apparatus of claim 1 further comprising a third comparator having a first input that receives a third threshold, said third threshold between said first threshold and said second threshold, said third comparator having a second input that receives said input signal.
3. The apparatus of claim 2 wherein said third threshold is a primary threshold.
4. The apparatus of claim 2 wherein said third threshold is midway between said first threshold and said second threshold.
5. The apparatus of claim 1 further comprising an offset compensation loop unit that positions said first threshold above an offset of said input signal and positions said second threshold below said offset of said input signal by presenting a sequence of error terms to an accumulator in response to said detection.
6. The apparatus of claim 5 wherein said error terms have the same magnitude.
7. The apparatus of claim 5 wherein said detection is communicated from said offset detection unit to said offset compensation loop unit by either of a pair

of signals, a first of said signals indicative of said input signal being above said first threshold, a second of said signals indicative of said input signal being below said second threshold.

8. The apparatus of claim 1 further comprising a sample delay unit input coupled to an output of said first comparator.
9. The apparatus of claim 8 further comprising a correlation unit coupled to an output of said sample delay unit.
10. The apparatus of claim 9 further comprising a register that holds a predetermined data pattern, said register coupled to said correlation unit.
11. The apparatus of claim 1 further comprising a demodulator output coupled to said second inputs of said comparators.
12. The apparatus of claim 11 further comprising a sample and hold circuit between said demodulator and said second inputs of said comparators.
13. An apparatus, comprising:
  - a) a first comparator having a first input that receives a first threshold and a second input that receives an input signal;
  - b) a second comparator having a first input that receives a second threshold, said second threshold less than said first threshold, said second comparator having a second input that receives said input signal;
  - c) a third comparator having a first input that receives a third threshold, said third threshold between said first threshold and said second threshold, said third comparator having a second input that receives said input signal; and
  - d) an offset sensing unit that detects said input signal above said first threshold or below said second threshold by comparing said first and second comparator outputs.
14. The apparatus of claim 13 wherein said third threshold is a primary threshold.

15. The apparatus of claim 14 wherein said third threshold is midway between said first threshold and said second threshold.
16. The apparatus of claim 13 further comprising an offset compensation loop unit that positions said first threshold above an offset of said input signal and positions said second threshold below said offset of said input signal by presenting a sequence of error terms to an accumulator in response to said detection.
17. The apparatus of claim 16 wherein said error terms have the same magnitude.
18. The apparatus of claim 16 wherein said detection is communicated from said offset detection unit to said offset compensation loop unit by either of a pair of signals, a first of said signals indicative of said input signal being above said first threshold, a second of said signals indicative of said input signal being below said second threshold.
19. The apparatus of claim 16 wherein said offset compensation loop unit further comprises a first bandwidth and a second bandwidth, said first bandwidth greater than said second bandwidth, said offset compensation loop unit employing said first bandwidth if said detection occurs, said offset compensation loop unit employing said second bandwidth if said detection does not occur.
20. The apparatus of claim 19 wherein said offset compensation loop unit further positions, when employing said second bandwidth, said third threshold at said input signal offset by taking the difference between said third comparator output signal and 0.5 to generate a second sequence of error terms.
21. The apparatus of claim 20 wherein said second sequence of error terms have magnitudes less than the magnitude of said sequence of error terms.
22. The apparatus of claim 19 wherein said offset compensation loop unit further positions, when employing said second bandwidth, said third threshold at

said input signal offset by taking the difference between the average of said third comparator output signal and 0.5 to generate a second sequence of error terms.

23. The apparatus of claim 22 wherein said second sequence of error terms have magnitudes less than the magnitude of said sequence of error terms.

24. The apparatus of claim 16 wherein said offset compensation loop unit further comprises a third bandwidth, said third bandwidth less than said second bandwidth, said offset compensation loop unit employing said third bandwidth after a preamble is detected.

25. The apparatus of claim 13 further comprising a sample delay unit input coupled to an output of said third comparator.

26. The apparatus of claim 25 further comprising a correlation unit coupled to an output of said sample delay unit.

27. The apparatus of claim 26 further comprising a register that holds a predetermined data pattern, said register coupled to said correlation unit.

28. The apparatus of claim 27 wherein said predetermined data pattern corresponds to a preamble for a BLUETOOTH packet.

29. The apparatus of claim 13 further comprising a demodulator output coupled to said second inputs of said comparators.

30. The apparatus of claim 29 further comprising a sample and hold circuit between said demodulator and said second inputs of said comparators.

31. The apparatus of claim 13 wherein said offset detection unit detects said input signal above said first threshold or below said second threshold by comparing said first, second and third comparator outputs.

32. A method, comprising:  
a) comparing an input signal against a first threshold and a second threshold to generate a first thresholded signal and a second thresholded signal, said first threshold higher than said second threshold; and

- b) detecting if said input signal is above said first threshold or below said second threshold by comparing said first and second thresholded signals.
33. The method of claim 32 wherein said detection is triggered if said first and second thresholded signals are equal.
34. The method of claim 33 wherein a signal indicative that said input signal is above said first threshold is generated if said first and second threshold signals are equal to 1.
35. The method of claim 33 wherein a signal indicative that said input signal is below said second threshold is generated if said first and second threshold signals are equal to 0.
36. The method of claim 32 further comprising storing samples of said first thresholded signal into a sample delay unit.
37. The method of claim 36 further comprising correlating said samples against a pre-determined pattern.
38. The method of claim 37 wherein said pre-determined pattern is a sequence of 0s.
39. The method of claim 37 wherein said pre-determined pattern is a sequence of 1s.
40. The method of claim 39 wherein the length of said sequence of 1s is greater than the length of a second sequence of 1s found in said first thresholded signal when said input signal has a symbol peak above said first threshold.
41. The method of claim 32 further comprising sending a signal to an offset compensation loop unit if said detection arises, said signal indicative of whether said input signal is above said first threshold or below said second threshold, said offset compensation loop unit having an output that controls said first and second thresholds.
42. The method of claim 41 further comprising generating a series of error terms in response to said signal.

43. The method of claim 42 wherein said error terms are added to adjust said offset compensation loop unit output.
44. The method of claim 41 further comprising comparing said input against a third threshold to generate a third thresholded signal, said third threshold between said first and second thresholds.
45. The method of claim 44 further comprising storing samples of said third thresholded signal into a sample delay unit.
46. The method of claim 45 further comprising correlating said samples against a pre-determined pattern.
47. The method of claim 47 wherein said pre-determined pattern corresponds to a BLUETOOTH packet preamble.
48. The method of claim 44 further comprising sending a second signal to said offset compensation loop unit indicative of whether a preamble within a packet has been found.
49. The method of claim 48 further comprising adjusting said first, second and third thresholds with a higher bandwidth if said signal is active and adjusting said first, second and third thresholds with a lower bandwidth if said signal is not active.
50. The method of claim 49 further comprising adjusting said first, second and third thresholds according to a first lower bandwidth if said preamble has not been found and a second lower bandwidth if said preamble has been found, said first lower bandwidth greater than said second lower bandwidth.
51. A method, comprising:
- a) adjusting a first, second and third thresholds with a feedback loop, said feedback loop having a first bandwidth if a signal is above said first threshold or below said second threshold, said third threshold below said first threshold and above said second threshold; and
  - b) adjusting said first, second and third thresholds with said feedback loop, said feedback loop having a second bandwidth if said signal is between said

first and second thresholds, said first bandwidth greater than said second bandwidth.

52. The method of claim 51 wherein said adjusting further comprises adding a sequence of error terms within said feedback loop to change an output level of said feedback loop.

53. The method of claim 52 further comprising converting said feedback loop output level from a digital representation to an analog voltage before applying said adjustment.

54. The method of claim 51 wherein each of said error terms further comprise a magnitude indicative of said adjusting amount.

55. The method of claim 54 wherein said error term magnitudes are greater when said feedback loop operates in said first bandwidth than when said feedback loop operates in said second bandwidth.

56. The method of claim 54 wherein said error term magnitudes are the same when said feedback loop operates in said first bandwidth.

57. The method of claim 54 wherein said second bandwidth further comprises a higher second bandwidth and a lower second bandwidth, said higher second bandwidth employed if a packet's pre-determined data pattern has not been found, said lower second bandwidth employed if said packet's pre-determined data pattern has been found.

58. The method of claim 57 wherein said packet's pre-determined data pattern is a BLUETOOTH preamble.

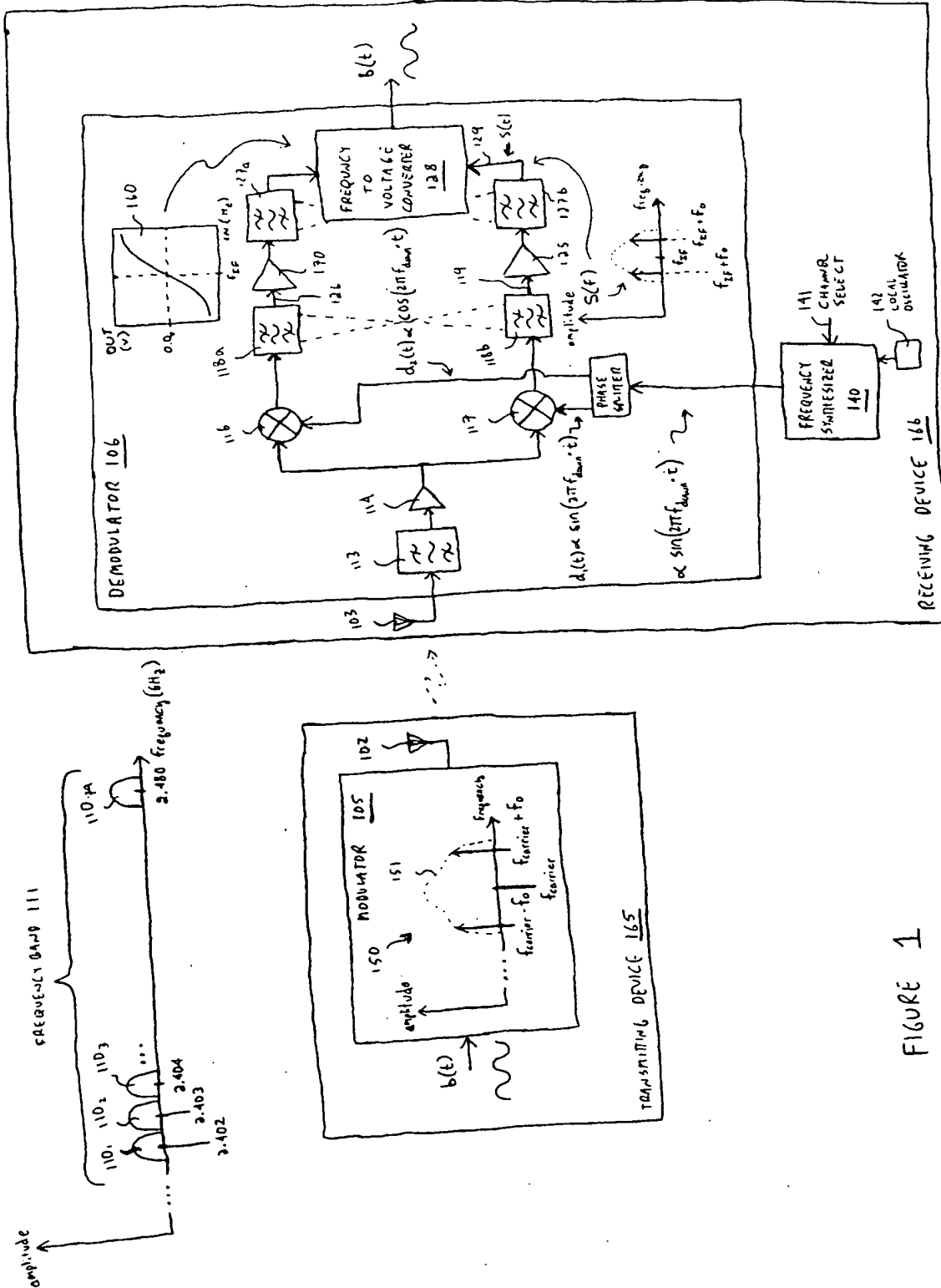


FIGURE 1

FIG 2A

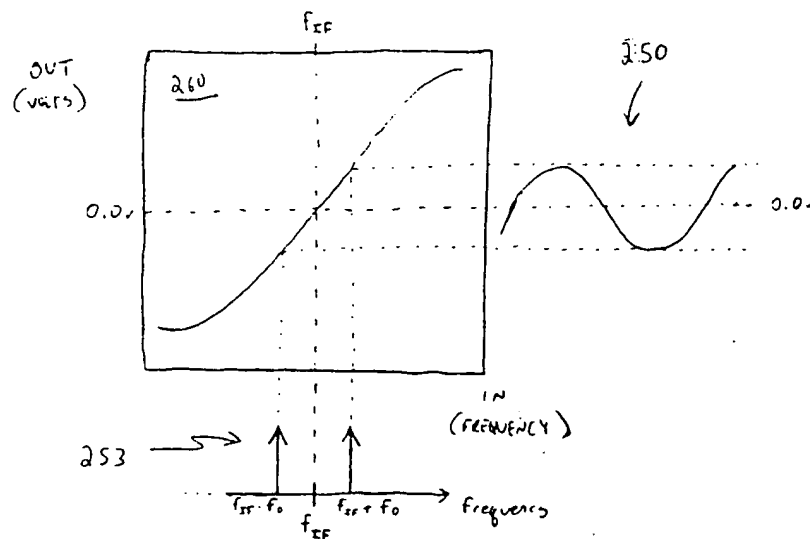
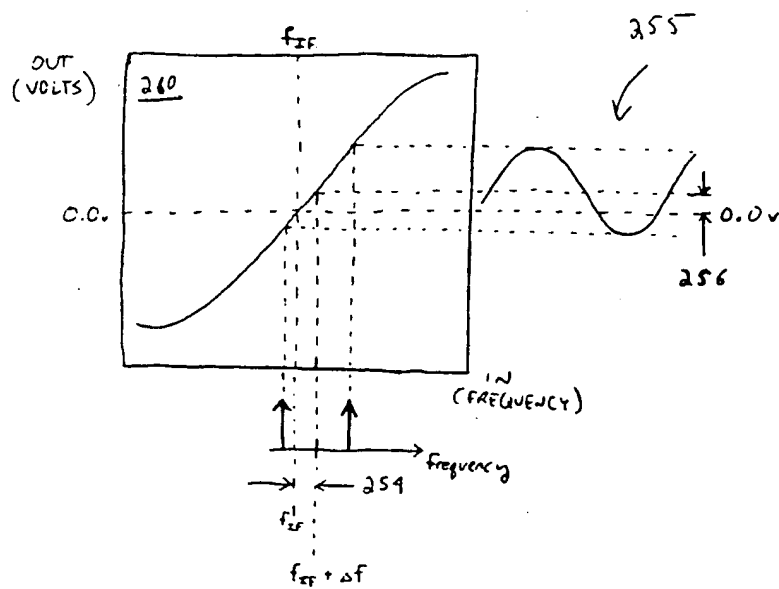


FIG 2B



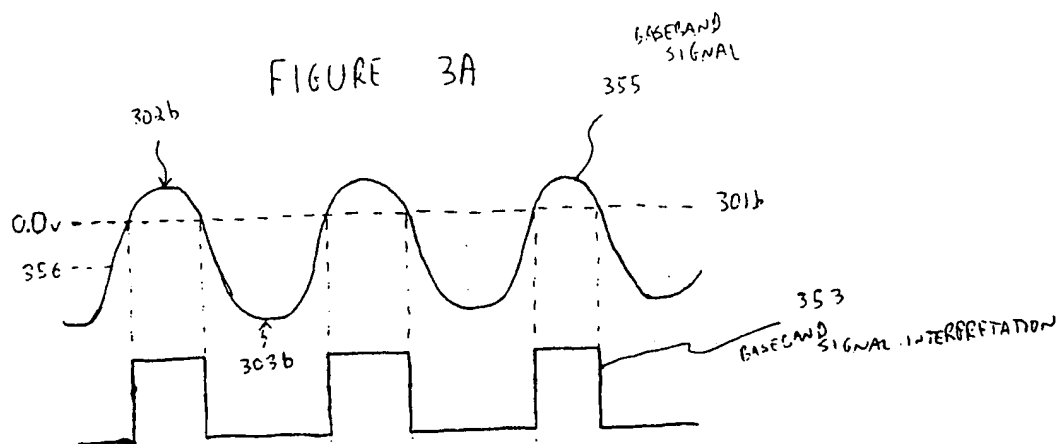
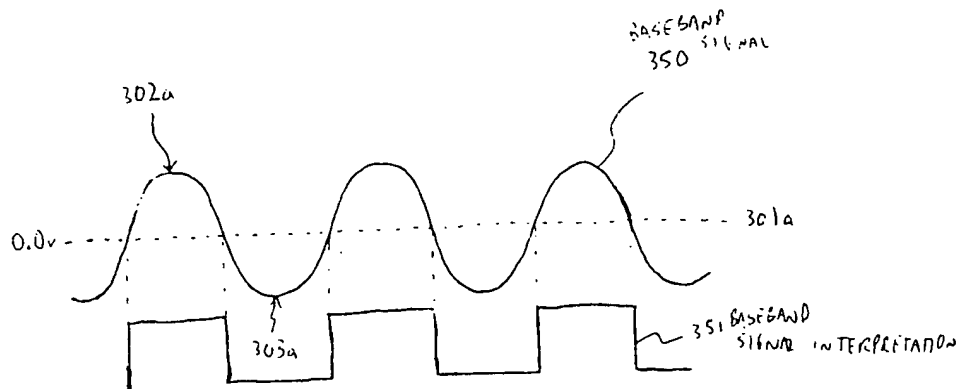


FIGURE 3B

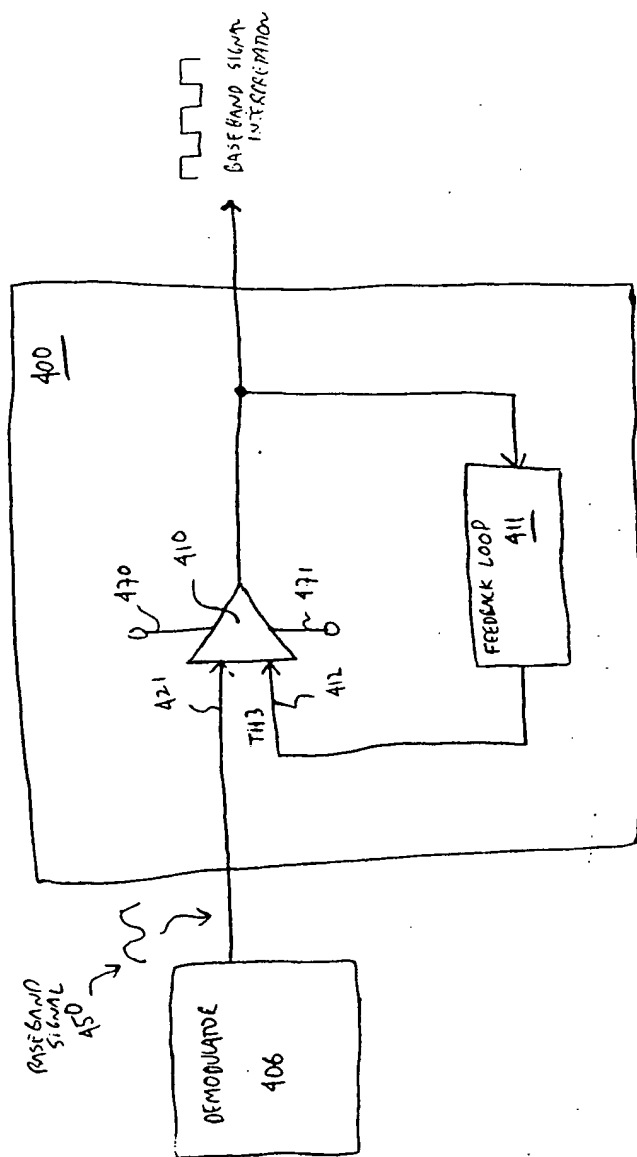


FIGURE 4

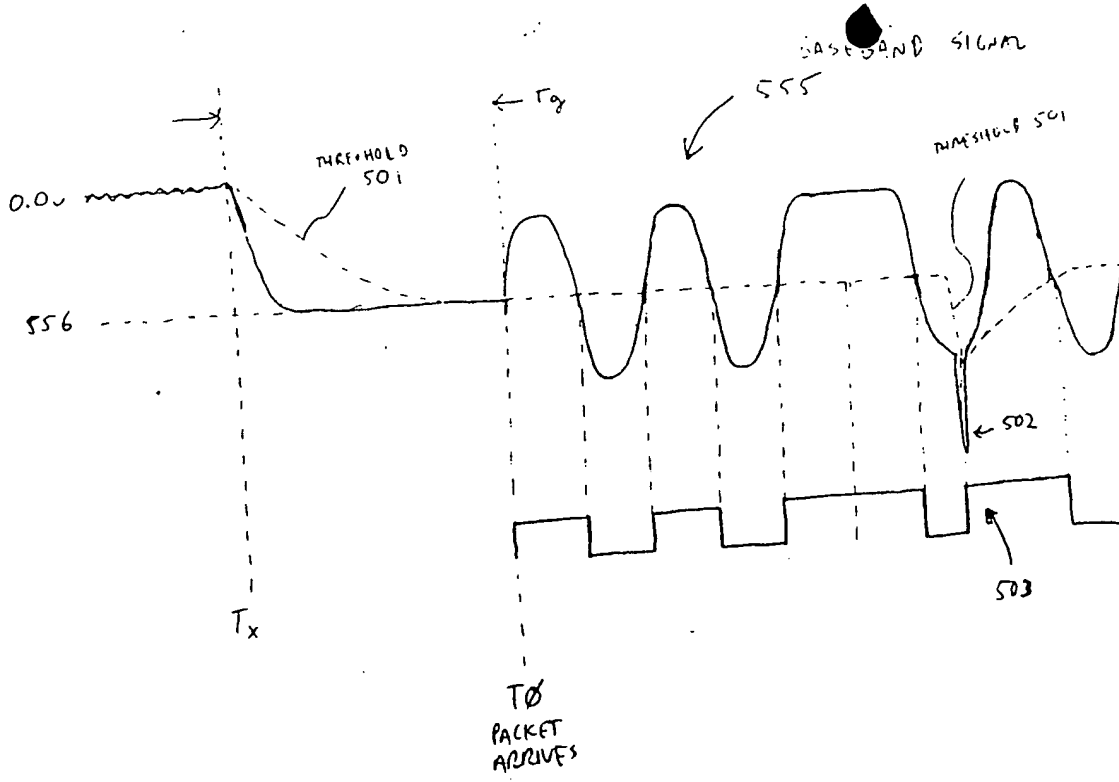


FIGURE 5

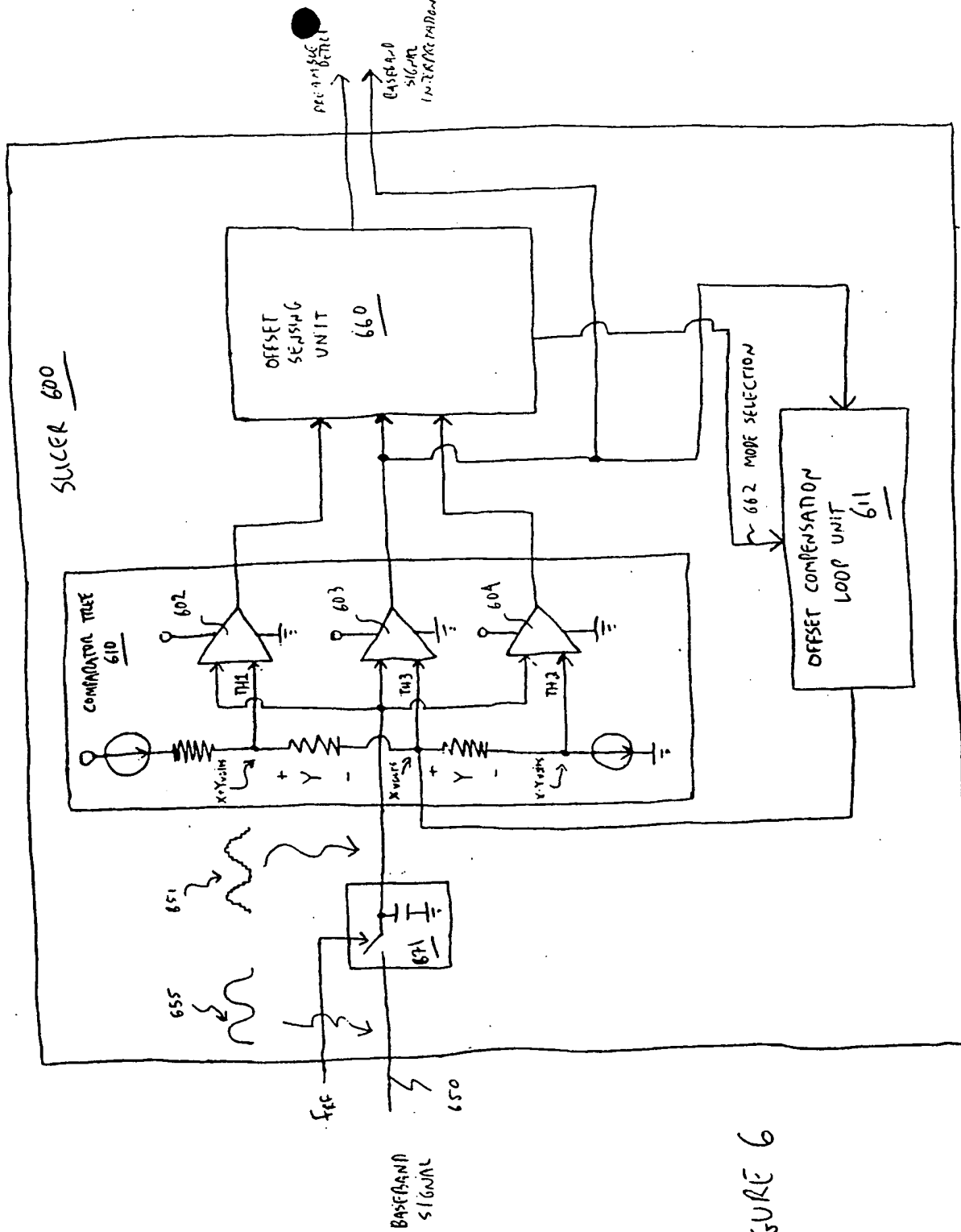


FIGURE 6

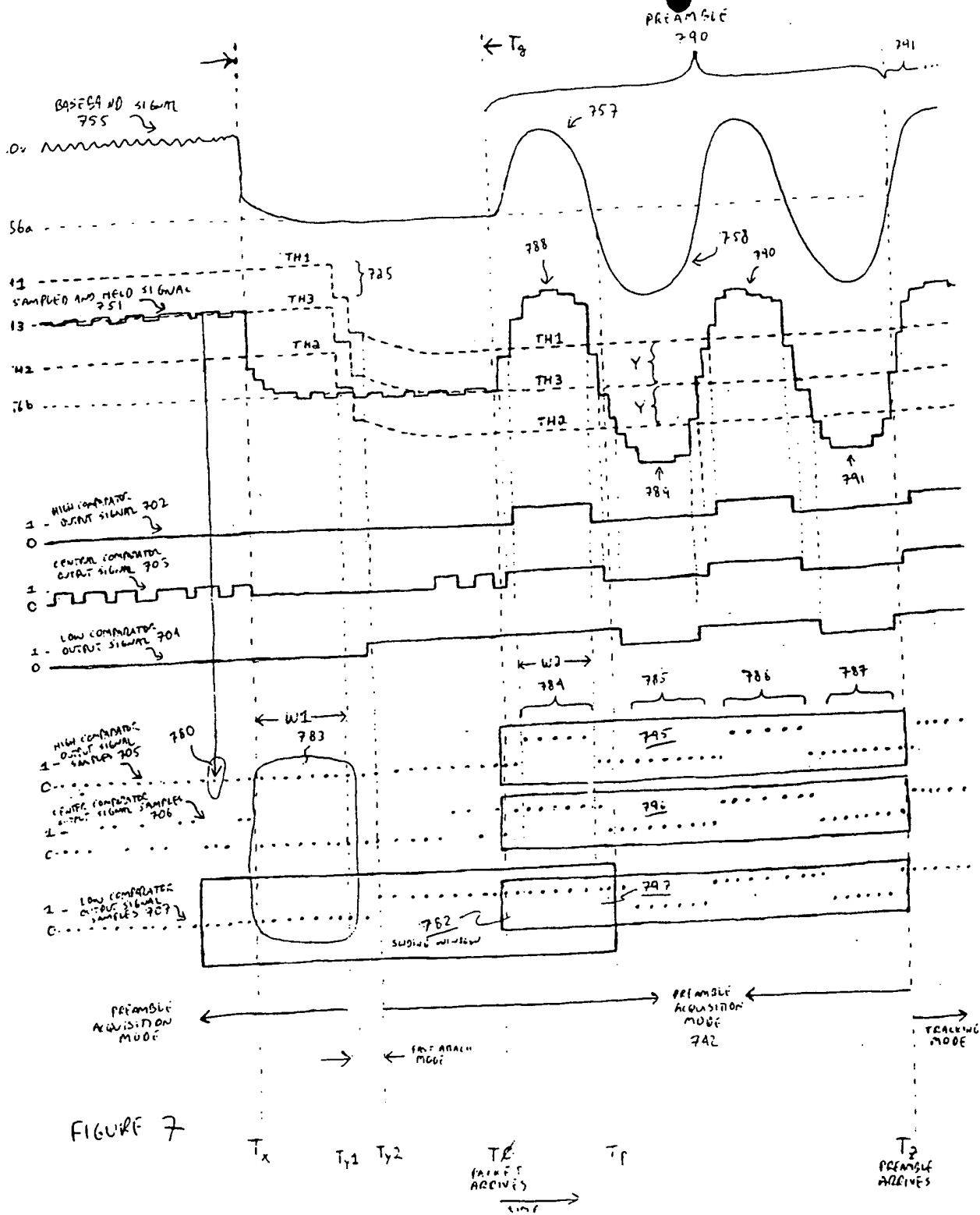


FIGURE 7

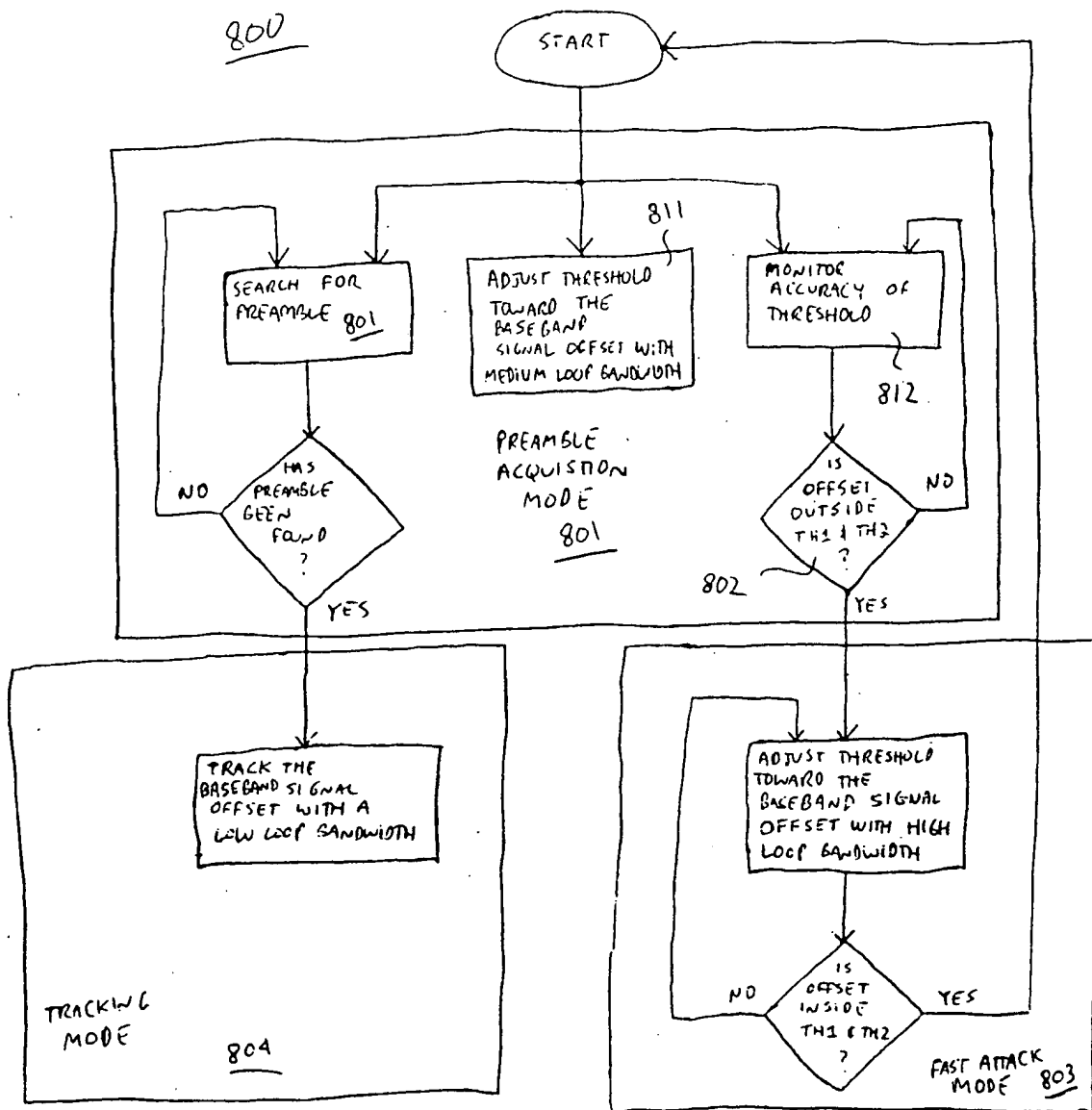


FIGURE 8

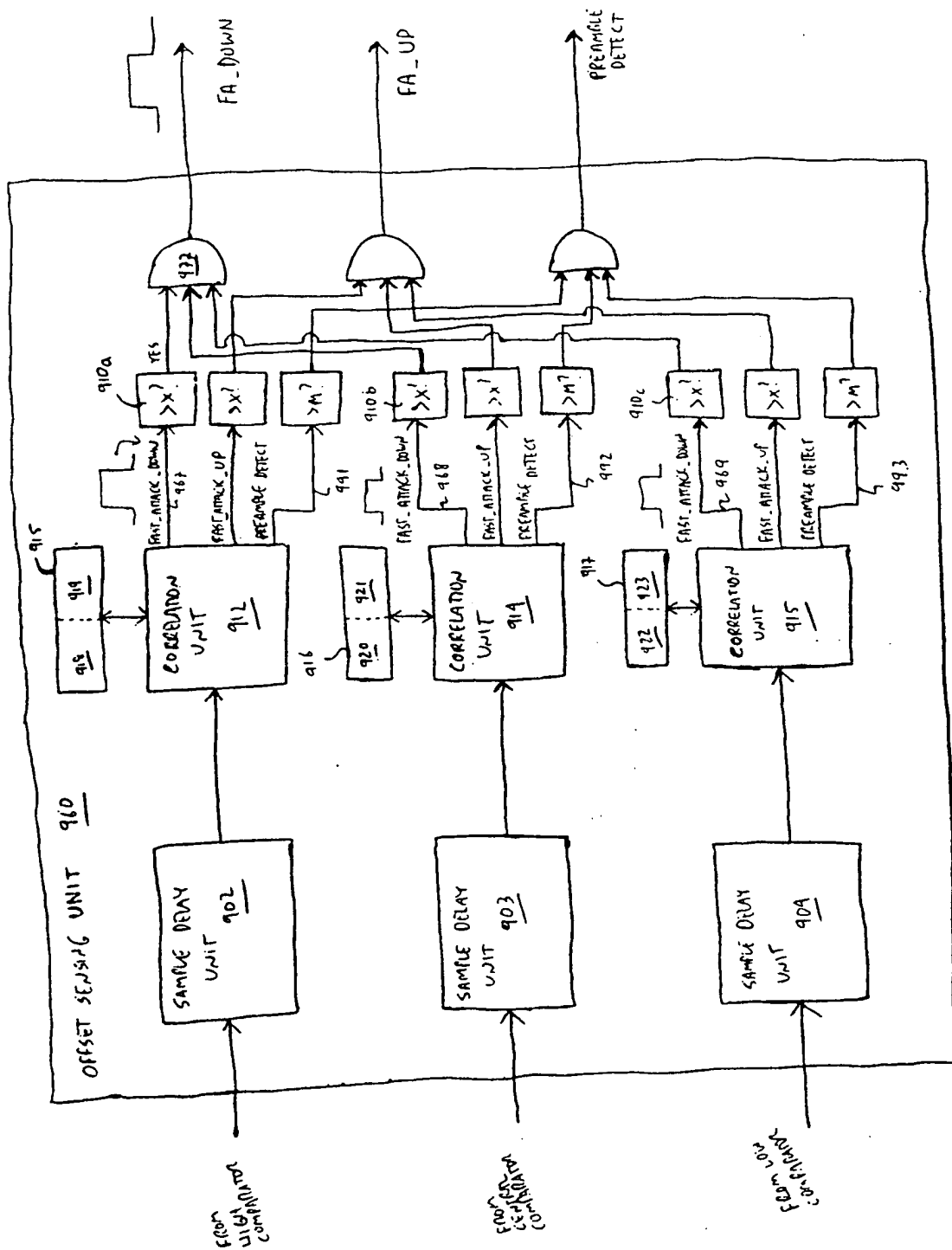


FIGURE 9

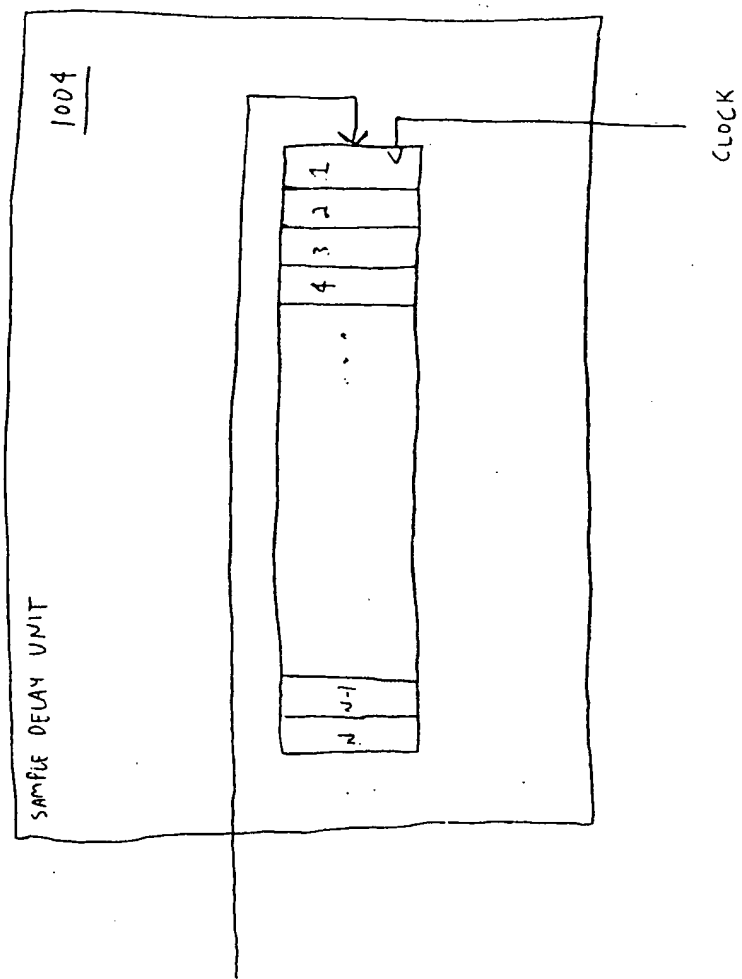


FIGURE 10

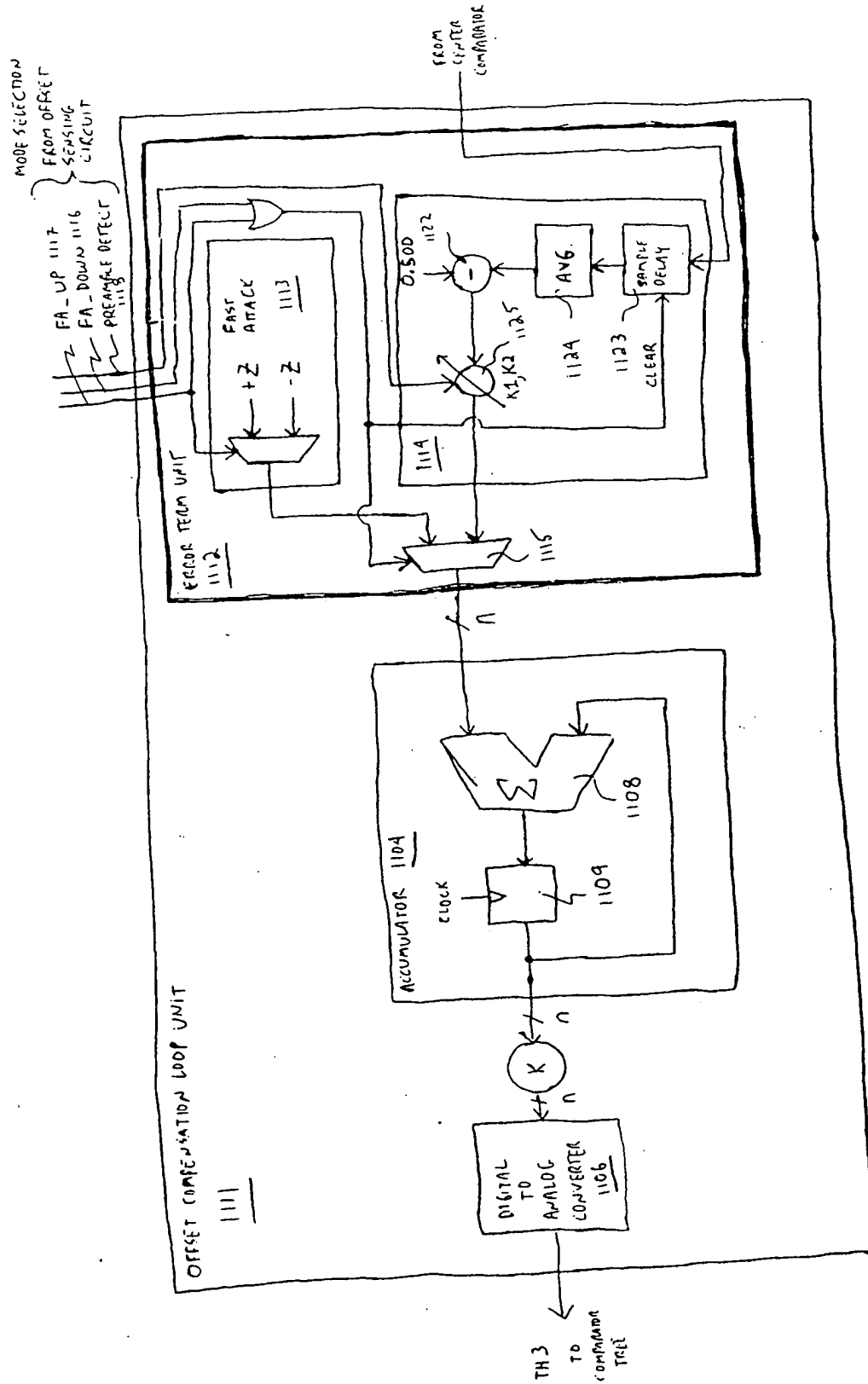


FIGURE 11

# INTERNATIONAL SEARCH REPORT

International application No. .  
PCT/US00/41025

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H04B 17/00  
US CL : 455/226.2; 375/272; 327/362; 341/126, 127, 132

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 455/67.1, 226.2, 226.4; 375/245, 272, 316, 317; 327/78, 80, 362; 341/120, 126, 127, 132

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
EAST

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,766,417 A (TAKAYAMA et al) 23 August 1988 (23.08.1988), column 1, line 31 - column 2, line 2.	1-55
A	US 5,262,686 A (KUROSAWA) 16 November 1993 (16.11.1993), column 3, line 50 - column 4, line 39.	1-55
A	US 5,412,687 A (SUTTON et al) 02 May 1995 (02.05.1995), column 6, line 5 - column 8, line 48.	1-55
A	US 5,661,4 A (VALLANCOURT) 26 August 1997 (26.08.1997), column 3, line 5 - column 6, line 6.	1-55

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

Special categories of cited documents:	
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"E" earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

22 January 2001

Date of mailing of the international search report

05 MAR 2001

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(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
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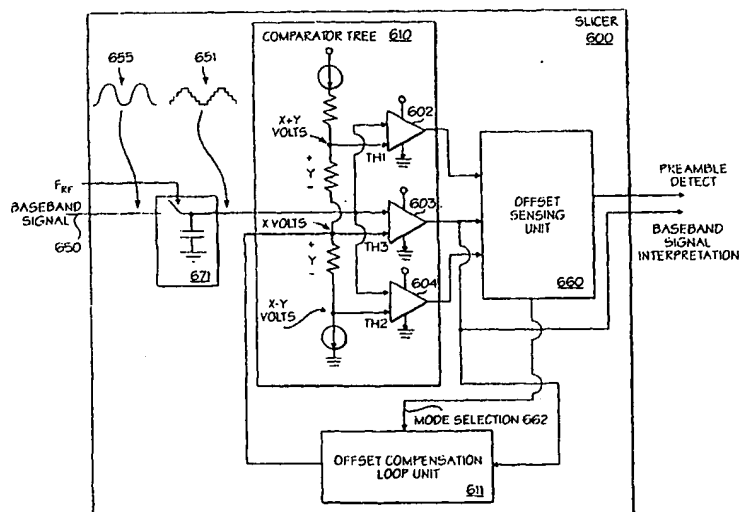
PCT

(10) International Publication Number  
WO 01/026260 A1

- (51) International Patent Classification<sup>7</sup>: H04B 17/00 (72) Inventor; and  
(75) Inventor/Applicant (for US only): O'BRIEN, Jeremiah, Christopher [II/IE]; Ballybawn East, Ballydehob, Co., Cork (IE).
- (21) International Application Number: PCT/US00/41025
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- (25) Filing Language: English
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(54) Title: METHOD AND APPARATUS FOR COMPARATOR TREE STRUCTURE FOR FAST ACQUISITION OF OFFSETS INDUCED IN A WIRELESS RECEIVER



(57) Abstract: A method that involves comparing an input signal (650) against a first threshold (TH1) and a second threshold (TH2) to generate a first thresholded signal and a second thresholded signal. The first threshold (TH1) is greater than the second (TH2) threshold. Then, detecting if the input signal (650) is above the first threshold (TH1) or below the second threshold (TH2) by comparing the first and second thresholded signals.

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## Method and Apparatus For Comparator Tree Structure For Fast Acquisition of Offsets Induced In A Wireless Receiver

### FIELD OF THE INVENTION

The field of invention relates to wireless receivers generally; and more specifically to a comparator tree structure that allows a receiver to quickly adjust to an offset in a baseband signal.

### BACKGROUND

#### Super Heterodyne and Frequency Shift Keyed (FSK) Modulation/Demodulation

Figure 1 shows a portion 106 of a receiving device 166 referred to as a demodulator. A demodulator 106 provides a signal (commonly referred to as a baseband signal  $b(t)$  in various applications) that is representative of the information being sent from a transmitting device 165 to a receiving device 166. The demodulator 106 extracts (i.e., demodulates) the baseband signal  $b(t)$  from a high frequency wireless signal that "carries" the baseband signal  $b(t)$  through the medium (e.g., airspace) separating the transmitting and receiving devices 165, 166.

The particular demodulator 106 example of Figure 1 is designed according to: 1) a demodulation approach that is commonly referred to as super heterodyne detection (hereinafter referred to as a heterodyne detection for simplicity); and 3) a modulation/demodulation scheme referred to as Frequency Shift Keying (FSK). The industry standard referred to as "BLUETOOTH" (the requirements of which may be found in "Specification of the Bluetooth System", Core v.1.0B, 12/1/99, and published by the Bluetooth Special Interest Group (SIG)) can apply to both of these approaches and, accordingly, will be used below as a basis for reviewing the following background material.

Heterodyne detection is normally used when dedicated channels are allocated within a range of frequencies 111 (where a range of frequencies may also be referred to as a "band" 111). For BLUETOOTH applications within the United

States, 89 channels  $110_1, 110_2, 110_3, \dots, 110_{79}$  are carried within a 2.400 GHz to 2.482 GHz band 111. Each of the 79 channels are approximately 1 Mhz wide and are centered at frequencies 1 Mhz apart.

The first channel  $110_1$  is centered at 2.402 Ghz, the second channel  $110_2$  is centered at 2.403 Ghz, the third channel  $110_3$  is centered at 2.404 Ghz, etc., and the seventy ninth channel  $110_{79}$  is centered at 2.480 Ghz. The heterodyne demodulator 106 accurately receives a single channel while providing good suppression of the other channels present within the band 111. For example, if channel  $110_2$  is the channel to be received, the baseband signal  $b(t)$  within channel  $110_2$  will be presented while the baseband signals carried by channels  $110_1$ , and  $110_3$  through  $110_{79}$  will be suppressed.

An FSK modulation/demodulation approach is commonly used to transmit digital data over a wireless system. An example of an FSK modulation approach is shown in Figure 1. A transmitting modulator 105 within a transmitting device 165 modulates a baseband signal at a carrier frequency  $f_{\text{carrier}}$  into an antennae 102. That is (referring to the frequency domain representation 150 of the signal launched into the antennae 102) if the baseband signal corresponds to a first logic value (e.g., "1"), the signal 150 has a frequency of  $f_{\text{carrier}} + f_o$ . If the data to be transmitted corresponds to a second logic value (e.g., "0"), the signal has a frequency of  $f_{\text{carrier}} - f_o$ .

Thus, the signal launched into the antennae 102 alternates between frequencies of  $f_{\text{carrier}} + f_o$  and  $f_{\text{carrier}} - f_o$  depending on the value of the data being transmitted. Note that in actual practice the transmitted signal 150 may have a profile 151 that is distributed over a range of frequencies in order to prevent large, instantaneous changes in frequency. The carrier frequency  $f_{\text{carrier}}$  corresponds to the particular wireless channel that the digital information is being transmitted within. For example, within the BLUETOOTH wireless system,  $f_{\text{carrier}}$  corresponds to 2.402 Ghz for the first channel  $110_1$ . The difference between the carrier frequency and the frequency used to represent a logical value is referred to as the deviation frequency  $f_o$ .

Referring now to the heterodyne demodulator 106, note that the signal received by antennae 103, may contain not only every channel within the frequency band of interest 111, but also extraneous signals (e.g., AM and FM radio stations, TV stations, etc.) outside the frequency band 111. The extraneous signals are filtered by filter 113 such that only the frequency band of interest 111 is passed. The filter 113 output signal is then amplified by an amplifier 114.

The amplified signal is directed to a first mixer 116 and a second mixer 117. A pair of downconversion signals  $d1(t)$ ,  $d2(t)$  that are  $90^\circ$  out of phase with respect to each other are generated. A first downconversion signal  $d1(t)$  is directed to the first mixer 116 and a second downconversion signal  $d2(t)$  is directed to the second mixer 117. Each mixer multiplies its pair of input signals to produce a mixer output signal. Note that the transmitting modulator 105 may also have dual out of phase signals that are not shown in Figure 1 for simplicity. Transmitting a pair of signals that are  $90^\circ$  out of phase with respect to one another conserves airborne frequency space by a technique referred to in the art as single sideband transmission.

The frequency  $f_{\text{down}}$  of both downconversion signals  $d1(t)$ ,  $d2(t)$  is designed to be  $f_{\text{carrier}} - f_{\text{IF}}$ . The difference between the downconversion frequency  $f_{\text{down}}$  and the carrier frequency  $f_{\text{carrier}}$  is referred to as the intermediate frequency  $f_{\text{IF}}$ . Because it is easier to design filters 118a,b and 127a,b that operate around the intermediate frequency, designing the downconversion that occurs at mixers 116, 117 to have an output term at the intermediate frequency  $f_{\text{IF}}$  enhances channel isolation.

The mixer 117 output signal may be approximately expressed as

$$kb_{\text{FSK}}(t)\cos(2\pi f_{\text{carrier}} t)\cos(2\pi f_{\text{down}} t). \quad \text{Eqn. 1}$$

Note that Equation 1 is equal to

$$kb_{\text{FSK}}(t)[\cos(2\pi (f_{\text{carrier}} - f_{\text{down}})t) + \cos(2\pi (f_{\text{carrier}} + f_{\text{down}})t)] \quad \text{Eqn. 2}$$

which is also equal to

$$kb_{\text{FSK}}(t)\cos(2\pi f_{\text{IF}} t) + kb_{\text{FSK}}(t)\cos(2\pi (f_{\text{carrier}} + f_{\text{down}})t) \quad \text{Eqn. 3}$$

using known mathematical relationships. The  $b_{\text{FSK}}(t)$  term represents a frequency shift keyed form of the baseband signal (e.g., a signal that alternates in frequency between  $+f_0$  for a logical "1" and  $-f_0$  for a logical "0"). The constant  $k$  is related to

the signal strength of the received signal and the amplification of amplifier 114. For approximately equal transmission powers, signals received from a nearby transmitting device are apt to have a large  $k$  value while signals received from a distant transmitting device are apt to have a small  $k$  value.

Equation 3 may be viewed as having two terms: a lower frequency term expressed by  $kb_{\text{FSK}}(t)\cos(2\pi f_{\text{IF}}t)$  and a higher frequency term expressed by  $kb_{\text{FSK}}(t)\cos(2\pi (f_{\text{carrier}} + f_{\text{down}})t)$ . Filter 118b filters away the high frequency term leaving the lower frequency term  $kb_{\text{FSK}}(t)\cos(2\pi f_{\text{IF}}t)$  to be presented at input 119 of amplification stage 125. Note that, in an analogous fashion, a signal  $kb_{\text{FSK}}(t)\sin(2\pi f_{\text{IF}}t)$  is presented at the input 126 of amplification stage 170.

Amplification stage 125 has sufficient amplification to clip the mixer 117 output signal. Filter 127b filters away higher frequency harmonics from the clipping performed by amplification stage 125. Thus, amplification stage 125 and filter 127b act to produce a sinusoidal-like waveform having approximately uniform amplitude for any received signal regardless of the distance (e.g.,  $k$  factor) between the transmitting device and the receiving device.

After filter 127, a signal  $s(t)$  corresponding to  $Ab_{\text{FSK}}(t)\cos(2\pi f_{\text{IF}}t)$  is presented to the frequency to voltage converter 128 input 129 (where  $A$  reflects the uniform amplitude discussed above). The spectral content  $S(f)$  of the signal  $s(t)$  at the frequency to voltage converter 128 input 129 is shown at Figure 1. The signal  $s(t)$  alternates between a frequency of  $f_{\text{IF}} + f_0$  (for a logical value of "1") and a frequency of  $f_{\text{IF}} - f_0$  (for a logical value of "0"). The spectral content  $S(f)$  of the signal  $s(t)$  at the frequency to voltage converter 128 input 129 is mapped against the transfer function 160 of the frequency to voltage converter 128 in order to reproduce the baseband signal  $b(t)$  at the demodulator output.

### Frequency Synthesis

Referring back to the pair of downconversion signals  $d1(t)$ ,  $d2(t)$  that are directed to mixers 116, 117, recall that the downconversion signals  $d1(t)$  and  $d2(t)$  should have a downconversion frequency  $f_{\text{down}}$  equal to  $f_{\text{carrier}} - f_{\text{IF}}$  for each of the channels 110<sub>1</sub> through 110<sub>79</sub>. For example, for an intermediate frequency  $f_{\text{IF}}$  of

3Mhz, the frequency synthesizer 140 is responsible for generating a frequency of 2.399 Ghz in order to receive the first channel 110<sub>1</sub> (i.e,  $f_{\text{carrier}} - f_{\text{IF}} = 2.402 - 0.003 \text{ Ghz} = 2.399 \text{ Ghz}$ ); a frequency of 2.400 Ghz in order to receive the second channel 110<sub>2</sub>; a frequency of 2.401 Ghz in order to receive the third channel 110<sub>3</sub>; . . . etc., and a frequency of 2.477 Ghz in order to receive the 79<sup>th</sup> channel 110<sub>79</sub>. A channel select input 141 presents an indication of the desired channel to the frequency synthesizer 140.

Both the transmitting device 165 and the receiving device 166 typically have a frequency synthesizer. A frequency synthesizer 140 is shown in the receiving device 166 (but not the transmitting device 165 for simplicity). Frequency synthesizers typically create their output signals by multiplying a reference frequency (such as the frequency of a local oscillator). As seen in Figure 1, frequency synthesizer 140 multiplies the frequency of local oscillator 142 to produce downconversion signals d1(t) and d2(t). For example, for a local oscillator 142 reference frequency of 13.000 MHz, frequency synthesizer 140 should have a multiplication factor of 184.53846 to produce downconversion signals d1(t), d2(t) used to receive the first channel 110<sub>1</sub> (i.e.,  $184.53846 \times 13.000 \text{ MHz} = 2.399 \text{ GHz}$ ).

A problem with wireless technology involves deviation from the "designed for" carrier  $f_{\text{carrier}}$  and/or downconversion  $f_{\text{down}}$  frequencies (e.g., from non zero tolerances associated with the local oscillator 140 reference frequency). As either (or both) of the carrier and/or downconversion frequencies deviate from their "designed for" values, offsets may be observed in the baseband signal b(t) at the demodulator 106 output.

Figure 2a shows a baseband signal 250 if the carrier and downconverting frequencies are ideal. As discussed above, the spectral content 253 of the signals produced by filters 127a,b will be centered at the intermediate frequency  $f_{\text{IF}}$ . Since the origin 250 of the frequency to voltage converter transfer curve 260 is centered at the intermediate frequency  $f_{\text{IF}}$ , the output signal 250 has no offset (e.g., has an offset positioned at 0.0volts)

Errors in the carrier and/or downconversion frequency, however, will cause the spectral content of the signals produced by filters 127a,b to be centered at an offset 254 from the intermediate frequency  $f_{IF}$ . That is, because  $f_{IF}$  in equation 3 corresponds to  $f_{carrier} - f_{down}$ , if either  $f_{carrier}$  or  $f_{down}$  (or both) are in error the value of  $f_{IF}$  in equation 3 does not correspond to the designed for  $f_{IF}$  value (e.g., 3Mhz) that is centered at the origin of the transfer curve 260. As such, the baseband signal 255 will have an offset 256 with respect to 0.0volts.

## SUMMARY OF INVENTION

A method that comprises comparing an input signal against a first threshold and a second threshold to generate a first thresholded signal and a second thresholded signal. The first threshold is greater than the second threshold. Then, detecting if the input signal is above the first threshold or below the second threshold by comparing the first and second thresholded signals.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the Figures of the accompanying drawings in which:

**Figure 1** shows an embodiment of a demodulator;

**Figure 2a** shows a baseband signal without an offset;

**Figure 2b** shows a baseband signal with an offset;

**Figure 3a** shows a proper baseband signal interpretation;

**Figure 3b** shows an improper baseband signal interpretation;

**Figure 4** shows an embodiment of a comparator having its threshold determined through a feedback loop;

**Figure 5** shows an exemplary portion of a packet as received from a demodulator;

**Figure 6** shows an embodiment of a slicer that can adjust its threshold to the offset of the signal shown in Figure 5;

**Figure 7** shows exemplary signaling associated with the slicer embodiment of Figure 6;

**Figure 8** shows a methodology executed by the slicer embodiment of Figure 6;

Figure 9 shows an exemplary embodiment of the offset sensing unit of Figure 6; Figure 10 shows an exemplary embodiment of a sample delay unit; and Figure 11 shows an exemplary embodiment of the offset compensation loop unit of the slicer shown in Figure 6.

#### DETAILED DESCRIPTION

A method is described that involves comparing an input signal against a first threshold and a second threshold to generate a first thresholded signal and a second thresholded signal. The first threshold is greater than the second threshold. Then, detecting if the input signal is above the first threshold or below the second threshold by comparing the first and second thresholded signals.

Another method is described that involves adjusting a first, second and third thresholds with a feedback loop. The feedback loop has a first bandwidth if a signal is above the first threshold or below the second threshold. The third threshold is below the first threshold and above the second threshold. The first, second and third thresholds are then adjusted by the feedback loop where the feedback loop has a second bandwidth if the signal is between the first and second thresholds. The first bandwidth is greater than the second bandwidth.

An apparatus is described of a first comparator having a first input that receives a first threshold and a second input that receives an input signal. The apparatus further comprises a second comparator having a first input that receives a second threshold where the second threshold is less than the first threshold. The second comparator also has a second input that receives the input signal. An offset sensing unit detects whether the input signal is above said first threshold or below said second threshold by comparing the first and second comparator outputs.

The method and apparatus described above, as well as other methods and apparatus, are discussed in more detail below.

Figure 3a shows a baseband signal 350 without an offset (similar to signal 250 of Figure 2b) while Figure 3b shows a baseband signal with an offset (similar to signal 255 of Figure 2b). As shown in Figure 3a, the determination as to whether or

not the baseband signal 350 corresponds to a logical 1 or a logical 0 depends upon the level of the baseband signal 350 with respect to a threshold 301a.

If the baseband signal 350 is above the threshold 301, the baseband signal is interpreted as a logical 1, if the baseband signal 350 is below the threshold 301, the baseband signal is interpreted as a 0. This activity may be referred to as thresholding, slicing, comparing and the like. Threshold level 301a shown in Figure 3 is properly positioned approximately midway between the positive and negative peaks 302a, 303a of the baseband signal 350. As a result, a correct digital interpretation 351 (e.g., having a 50% duty cycle) of the baseband signal 350 is formed as seen in Figure 3a. Note that the digital interpretation 353 of the baseband signal 350 is also commonly referred to as the baseband signal 353.

Referring to Figure 3b, if circuitry that performs the above described interpretation (typically referred to as a slicer or comparator) is unable to adjust (or unable to rapidly adjust) its threshold level 301b to an offset 356 in the baseband signal 355, the baseband signal 355 will be thresholded against an incorrect level (i.e., a level that is not approximately midway between the positive and negative peaks 302b, 303b of the baseband signal 355). An incorrect thresholding level 301b results in an incorrect digital interpretation 353 (e.g., excessive duty cycle distortion) as seen in Figure 3b.

For balanced coding schemes (i.e., schemes that transport data with an approximately equal number of 1s and 0s), such as those used within BLUETOOTH (as well as other wireless technology environments), the appropriate threshold level for a baseband signal may be determined by averaging the baseband signal. That is, referring to Figure 3b, the average value of the baseband signal (which is equal to its offset 356) is midway between the signal's positive and negative peaks 302b, 303b.

Figure 4 show a slicer embodiment 400 that is configured to automatically adjust its threshold level to the offset of the baseband signal by effectively averaging the slicer 400 output signal. The averaged demodulator 406 output signal is then applied as the threshold level of the slicer. The embodiment of

Figure 4 employs a comparator 410 that compares the baseband signal 450 at a first input 421 against a threshold at a second input 412. If the baseband signal 450 is greater than the threshold, the comparator 410 output is a logic "1". If the baseband signal is less than the threshold, the comparator 410 output is a logic "0".

Prior art receiving channels typically place an A/D converter and a slicer in series with one another after the demodulator output. That is, in prior art solutions, the baseband signal 450 is first converted from the analog domain to the digital domain by an A/D converter. The A/D converter produces a word of  $n$  bits (e.g., 6 bits) having a value representative of the baseband signal amplitude. The slicer then converts each A/D converter output word into a binary value (i.e., a "1" or "0") by comparing against a digital word that is representative of the threshold level.

Note that the approach of Figure 4 does not require an A/D converter between the demodulator 406 output and the slicer 400 input. That is, an analog comparator 410 may be used. The analog comparator 410 swings its output signal to the potential of either power rail (e.g., the supply node 470 potential for a logical "1" or the ground node 471 potential for a logical "0") depending upon the result of the comparison.

This approach may result in less expensive hardware costs because a binary interpretation of the baseband signal is obtained without the use of an A/D converter. In alternate embodiments, A/D conversion may be performed between the demodulator output and the comparator 410 input. As such, in these embodiments, the comparators 410 may be implemented as digital comparator.

For convenience, the term "baseband signal" and the like should be construed to cover either of these approaches. That is, the term "baseband signal" and the like should be construed as including an analog representation of the baseband signal or a digital representation of the baseband signal. Furthermore, the term "baseband signal" may be used to describe the input signal to a comparator regardless if the signal is the actual output of a demodulator 406 or the output some other functional block (such as a filter, A/D converter, etc.) that

processes the demodulator 406 output signal prior to the comparator. It is also important to point out that demodulator 406 may correspond to the demodulator design 106 of Figure 1 or another demodulator design different than the design shown in Figure 1.

In the slicer embodiment of Figure 4, a feed back scheme is used to control the comparator's threshold. The feed back loop 411 effectively averages the comparator 410 output signal in order to automatically adjust the comparator threshold level TH3 to the offset of the baseband signal 450. Details concerning possible embodiments of the feed back loop 411 are provided in more detail below.

A matter of concern is the speed at which the feedback loop 411 adjusts the slicer's threshold level. The term "loop bandwidth" may be used to refer to how quickly a feedback loop 411 can change a slicer's threshold level. A higher loop bandwidth corresponds to the ability to change the threshold level at a faster rate. Generally, during the initial moments of a received signal, more accurate comparator interpretations of the baseband signal 450 are achieved as the loop bandwidth increases.

Figure 5 demonstrates this property in more detail. Figure 5 shows a baseband signal 555. In Figure 5, a packet of information (hereinafter "a packet") sent by a transmitting device arrives at the receiving device at time T0. A corresponding offset 556 in the baseband signal 555 is observed (e.g., as caused by frequency synthesis inaccuracies that exist within the transmitting and/or receiving devices). Note that a grace period Tg may exist between the moment that a packet actually arrives T0 and the moment Tx that a change in offset is first observed.

This grace period Tg typically results from a latency designed into the transmitting device between the moment that the carrier frequency  $f_{\text{carrier}}$  begins to be transmitted and the moment the baseband signal (i.e., the packet) begins to be modulated (i.e., transmitted). Typically, in order to ensure that the entire packet is reliably sent, the transmission of the baseband signal is delayed by Tg after the carrier frequency  $f_{\text{carrier}}$  is enabled. It is important to point out, however, that the

teachings discussed herein are applicable to environments where no such latency exists (i.e., where  $T_g = 0$ ).

In order to accurately interpret the received packet, the slicer should rapidly adjust its threshold 501 to the baseband signal offset 556 by the time the grace period  $T_g$  expires. That is, referring back to Figure 4, the feedback loop 411 should have a sufficiently high bandwidth so that it can quickly respond to the change in offset.

By the nature of electronic circuits, however, the faster the loop is able to respond to an offset in the baseband signal (i.e., the higher the loop bandwidth), the more susceptible the slicer is to noise in the baseband signal during subsequent interpretations. That is, a slicer having high loop bandwidth tends to undesirably change its threshold in response to any noise spikes (e.g., noise spike 502) that appear on the baseband signal 555.

The change in threshold in response to a noise spike 502 can cause an incorrect interpretation 503 of the baseband signal 555 as seen in Figure 5. Slicers configured with a low loop 411 bandwidth have better immunity to noise. In a sense, because a low loop bandwidth is less capable of sudden threshold changes, the noise spike 502 exists for too brief a moment of time for the feedback loop (and therefore the threshold level) to respond to it.

An approach that enhances the overall interpretation of the baseband signal involves adjusting the feedback loop bandwidth in light of the difference between the offset 556 in the baseband signal and the slicer's threshold 501. Specifically, the loop bandwidth is increased as the difference between the threshold and the baseband signal offset increases.

Thus, if a large offset appears when a transmitting device begins to transmit to the receiving device, the slicer can rapidly adjust its threshold to the offset. After the threshold is rapidly corrected for, the slicer "switches over" to a smaller loop bandwidth that provides sufficient noise immunity during subsequent interpretations of the baseband signal 555.

This approach implies the presence of two functions. First, the ability to detect the proximity of the current thresholding level to the offset of the baseband signal. Second, the ability to calculate thresholds with different loop bandwidths in light of this detection. Both of these aspects are discussed immediately below.

Figure 6 shows a slicer embodiment 600 aimed at achieving the interpretation approach described just above. The slicer embodiment 600 includes a comparator tree 601, an offset sensing unit 660 and a feedback loop 611 that can operate at different loop bandwidths. The feedback loop 611 may also be referred to as an offset compensation loop 611 or offset compensation loop unit 611. The comparator tree 601 of Figure 6 provides a plurality of signals that may be analyzed in order to detect the proximity/remoteness of the slicer threshold to/from the baseband signal offset.

The comparator tree 601 has a plurality of comparators 602, 603, 604 that threshold (i.e., compare) a common input signal against different threshold levels. For example, as seen in the embodiment of Figure 6, three comparators 602, 603, 604 threshold a common input signal 651 against three different threshold levels a first threshold level TH1, a second threshold level TH2 and a third threshold level TH3. The thresholds may be established, as seen in Figure 6, by running a fixed current from a current source through a series of resistors. In an embodiment,

In various embodiments the threshold levels may be set equidistant from one another. For example, as seen in Figure 6, if the central threshold level TH3 corresponds to X volts, the upper TH1 and lower TH2 thresholding levels correspond to X+Y volts and X-Y volts respectively. As such, each threshold level is separated from its neighboring threshold level(s) by Y volts. In an embodiment, a resistor value of 1kohm and a current of 100 micro-amp are utilized to establish a threshold separation Y of 0.1 volts.

Embodiments employing an odd number of comparators (such as the exemplary embodiment of Figure 6) may use the centrally located threshold level (such as threshold level TH3 in Figure 6) as the "main" or "primary" threshold level. A main/primary threshold level is the threshold level against which the

baseband signal is actually interpreted. For example, if the interpretation provided by the comparator 603 is used to by circuitry downstream from the slicer.

The offset sensing unit 660 monitors the outputs of the comparator tree 601 to gauge the accuracy of the threshold. The offset sensing unit 660 provides the offset compensation loop 611 with a mode input 662 that controls the bandwidth of the offset compensation loop 611. In the embodiment of Figure 6, the mode provided by the offset sensing unit 660 is indicative of the difference between the primary slicer threshold level TH3 and the baseband signal offset.

For example, if the offset sensing unit 660 determines that the primary threshold TH3 is sufficiently inaccurate such that a rapid threshold adjustment is desired, the mode input 662 indicates to the offset compensation loop 611 that a high loop bandwidth should be used. Similarly, if the offset sensing unit 660 determines that the present threshold is sufficiently accurate, the mode input 662 indicates to the offset compensation loop 611, 612 that a lower loop bandwidth should be used.

The offset compensation loop 611 determines, according to the mode presented by the offset sensing unit 660, a threshold for the baseband signal and applies the threshold to the comparator tree 601. Note that in the embodiment of Figures 6a the offset compensation loop 611 applies the main threshold TH3 to a central comparator 602 and the outer thresholds TH1 and TH2 are formed by level shifting Y volts above and below the main threshold TH3.

It is important to note that, although the embodiment of Figure 6 only shows a comparator tree having three comparators 601, 602, 603, other embodiments may use a different number of comparators. Increasing the number of comparators generally increases the resolution at which the difference between a threshold and the baseband signal may be detected. Many designers may choose to use an odd number of comparators (e.g., 3, 5, 7, etc.) so that the centrally located comparator receives a primary threshold. Applying a primary threshold to a central comparator is not a strict requirement, however. Comparator trees having an even number of comparators are also possible.

Figure 7 shows signals associated with the slicer embodiment 600 of Figure 6. In Figure 7, similar to Figure 5, a packet arrives at time  $T_0$ . A grace period  $T_g$  exists between the moment that the packet arrives  $T_0$  and the moment a change in offset first occurs  $T_x$ . Referring to Figures 6 and 7, the comparator tree 601 embodiment of Figure 6 receives an analog baseband signal 655, 755 at its input 650.

The analog input signal 655, 755 is "chopped" by a sample and hold circuit 671 to form a sampled and held signal 651, 751. The sampled and held signal 651, 751 is presented to each of the comparators 602, 603, 604. The sampled and held signal 651, 751 allows the baseband signal 655, 755 to be easily converted into a stream a binary values as seen in more detail below.

The sampled and held signal 671, 751 may still be viewed as an analog signal, thus analog comparators 602, 603, 604 are used in the comparator tree 601 embodiment of Figure 6. The analog comparators 602, 603, 604 each perform a comparison of the sampled and held signal 651, 751 against their respective thresholds  $TH_1$ ,  $TH_3$  and  $TH_2$ . Figure 7 shows the threshold levels  $TH_1$ ,  $TH_3$ ,  $TH_2$  superimposed upon the sampled and held signal 751 for ease of understanding the comparator tree operation.

The slicer embodiment 600 of Figure 6 may be specially configured to capture or otherwise identify the arrival of a pre-determined pattern. For example, in BLUETOOTH applications, the first four symbols of a BLUETOOTH packet (referred to as its preamble 790) are a "1010" pattern 790 as seen in Figure 7. By identifying the arrival of the preamble 790 at time  $T_z$ , the receiving device gains an understanding as to where in time the packet's data 791 following the preamble begins. The receiving device can then re-align the phase of its internal clocks to properly time the reception and processing of the packet's information 791.

In order to recognize the reception of the preamble, the slicer embodiment 600 of Figure 6 may be designed with a number of different modes and corresponding offset compensation loop bandwidths. For example, in one embodiment the slicer 600 employs three different modes that are described in

more detail below. Note, however, that the slicer embodiment 600 of Figure 6 may be designed to have more or less than three modes. Furthermore, before continuing, it should be understood that the slicer embodiment of Figure 6 may be designed to support other mechanisms for reliable packet interpretation (e.g., including those that do not need to recognize a "1010" preamble, but rather, some other pre-determined data pattern).

A first mode, referred to as a "fast attack" mode, is used if the difference between the baseband signal offset 756b and the primary threshold level TH3 is too large for reliable interpretation of the baseband signal. The "fast attack" mode employs the highest offset compensation loop 611 bandwidth in order to quickly remove the large difference between the baseband signal offset and the threshold level TH3.

A second mode, referred to as the "preamble acquisition mode" is used if the difference between the baseband signal offset 756b and the primary threshold level TH3 is small enough to allow for reliable detection of the packet's preamble. Because the primary threshold level TH3 is deemed accurate during the preamble acquisition mode, the preamble acquisition mode offset compensation loop 611 bandwidth is less than the fast attack mode offset compensation loop 611 bandwidth.

A third mode, referred to as "tracking mode" is used after the preamble 790 has been detected. The tracking mode has the lowest offset compensation loop 611 bandwidth. The tracking mode is used to interpret the baseband signal 755 for the remainder of the packet following the preamble 790. As such, it is designed to have better noise immunity than the other modes. Note that the preamble acquisition mode may further refine the accuracy of the primary threshold TH3 such that, by the time the preamble is detected (i.e., when the acquisition is first entered), only slight adjustments (if any) are made to the primary threshold level TH3 by the tracking mode.

Figure 8 shows a methodology 800 for the transition from one slicer mode to another slicer mode. The methodology 800 of Figure 8 adjusts the slicer's loop

bandwidth in response to the accuracy of the present primary threshold level TH3 and the amount of accuracy and/or bandwidth needed for the particular state of a packet's reception. The following discussion of the methodology 800 of Figure 8 refers to the sampled and held baseband signal 751 and the primary threshold level TH3 shown in Figure 7.

Referring to Figures 6, 7 and 8, the preamble acquisition mode 801 may be viewed as the default mode of the slicer prior to the arrival of a packet. As such, before the baseband signal 755 offset changes (at time Tx) as a result of the transmitting device's carrier frequency being enabled, the slicer is "looking and waiting" for the arrival of the packet's preamble 790 in preamble acquisition mode 801. Before time Tx, in preamble acquisition mode 801, the slicer: 1) searches 810 for a comparator tree 601 output pattern that corresponds to the preamble 790 (via the offset sensing unit 660 as described in more detail below); 2) adjusts 811 its threshold TH3 toward the offset 756b of the baseband signal 755 (via the offset compensation loop 611); and 3) monitors 812 the accuracy of the primary threshold level TH3 by examining the comparator tree 601 output signals (via the offset sensing unit 660 as described in more detail below).

Just after time Tx, the baseband signal 755 offset changes to a new level 756b as a result of the transmitting device's carrier frequency being enabled. The offset sensing unit 660 detects 802 the inaccuracy of the primary threshold level TH3 (as described in more detail below) at time Ty1 and changes the mode of the offset compensation loop 611 to the fast attack mode 803.

The fast attack mode 803, as described above, employs a high loop bandwidth and therefore rapidly adjusts 820 the slicer threshold TH3. In this example, a fixed correction amount 725 is "force fed" to the threshold value TH3 that rapidly moves the threshold TH3 in the proper direction. As a result large, discrete adjustments are made to the threshold TH3 during fast attack mode as seen in Figure 7. Discrete adjustments are made to the threshold TH3 (i.e., the slicer remains in fast attack mode 803) until the threshold TH3 reaches an acceptable degree of accuracy (as determined by the offset sensing unit 660 as

described in more detail below) with respect to the offset level 756b of the baseband signal.

When the acceptable degree of accuracy is achieved, at time Ty2 in Figure 7, the offset sensing unit 660 triggers the slicer's re-entry to preamble acquisition mode 801. After the slicer returns to the preamble acquisition mode 801 after Ty2, the offset compensation loop 611 further improves the accuracy of the threshold TH3 as seen in Figure 7.

The slicer 600 remains in preamble detection mode 801 until the preamble 790 is detected by the offset sensing unit 660 (as described in more detail below) at time Tz. After the preamble is detected (i.e., after time Tz), the slicer enters tracking mode 804. The slicer output (i.e., from central comparator 602 in the embodiment of Figure 6) is presented to downstream circuitry so that information within the packet 741 following the preamble 790 can be processed. The offset sensing unit 660 can also provide the arrival of the packet (e.g., time T0 or time Tz as just two examples) to clock adjustment circuitry that adjusts the phase of the receiver's internal clocks.

Note that, because the preamble 790 is only four symbols wide (i.e., consumes a small amount of time), there is small likelihood that a noise spike will: 1) occur over the course of the preamble 790; and 2) have sufficient amplitude to disrupt the interpretation of the preamble 790. As such, the offset compensation loop 611 bandwidth used during preamble acquisition mode can afford to be greater than the offset compensation loop 611 bandwidth used during tracking mode.

Furthermore, the higher offset compensation loop 611 bandwidth associated with the preamble acquisition mode 801 (as compared to the tracking mode 804) provides the slicer 600 with enough bandwidth to quickly adjust for any inaccuracy in the threshold TH3 that remains after the rapid threshold adjustment performed by the fast attack mode 803. Thus, as described above, the slicer's offset compensation loop 611 bandwidth is reduced as the accuracy of the threshold TH3 improves.

Figure 7 shows the sampled and held signal 751 that is produced by the sample and hold circuit 671 of Figure 6. The sampled and held signal 751 is a common input signal that is presented to all three comparators 602, 603, 604 in the embodiment of Figure 6. The thresholds TH1, TH3 and TH2, as applied to the sampled and held signal, is also shown in Figure 7 superimposed upon the sampled and held signal 751.

The corresponding comparator output signals 702, 703, 704 are also shown in Figure 7. That is signal 702 corresponds to the output signal of comparator 602 which employs a threshold level of TH1, signal 703 corresponds to the output signal of comparator 603 which employs a threshold level of TH3, and signal 704 corresponds to the output signal of comparator 604 which employs a threshold level of TH2. These signals 702, 703, 704 help provide an understanding of the offset detection circuit 660 of Figure 6, a more detailed embodiment of which is shown in Figure 9.

In the offset sensing unit embodiment 960 of Figure 9, each comparator output is coupled to a sample delay unit 902, 903, 904. Thus, sample delay unit 902 is coupled to the output of comparator 602, sample delay unit 903 is coupled to the output of comparator 603 and sample delay unit 904 is coupled to the output of comparator 604.

Each sample delay unit 902, 903, 904 effectively queues samples from its corresponding comparator output signal. The number of comparator output samples stored in a sample delay unit 902, 903, 904 determines the size of a "sliding window" that effectively scans across the samples as they are taken from the comparator output. Figure 7 shows exemplary samples 705, 706, 707 taken from their corresponding comparator output signals. That is, sampling 705 is a series of samples taken from the first comparator 602 output signal 702, sampling 706 is a series of samples taken from the second comparator 603 output signal 703, and sampling 707 is a series of samples taken from the third comparator 604 output signal 704.

Samples are accumulated by effectively taking periodic "snapshots" of the comparator output signal value. For example, in the embodiment of Figure 7, the samples are taken at the same frequency  $f_{RF}$  that the switch in the sample and hold circuit 671 is modulated at. Thus, as seen in region 780 of sample stream 780 of Figure 7, the timing of each sample is aligned with the "held regions" of the sampled and held signal 751. That is, each comparator output signal sample is taken when the sample and hold circuit 671 holds the baseband signal 755.

Samples may be collected, for example, by clocking the value of the comparator output signal 702, 703, 704 into its corresponding sample delay unit 902, 903, 904. If the baseband signal symbol rate is known (e.g., 1.00 Mbit/s as in the case of BLUETOOTH), the frequency  $f_{RF}$  used to sample and hold the baseband signal and/or clock the comparator output samples into a sample delay unit may be a multiple of this rate (e.g., for 8:1 oversampling, an 8MHz frequency may be used).

Figure 10 shows an example of the sample delay unit 904 of Figure 9 embodied as a shift register 1004. A comparator output signal 704 value is clocked into the shift register 1004 input with each rising clock edge. Thus, each bit in the register corresponds to a comparator output signal sample. With each new rising clock edge, a new sample is taken (i.e., entered into the shift register in location 1) and the previous samples (i.e., the samples already existing in the shift register) move to the left one space. The leftmost sample (in location N) expires because it is over written by the sample value on its right. Collecting the samples in this manner corresponds to forming a sliding window that captures the most recent N samples of the comparator output signal (where N is the size of the register).

For example, as seen in Figure 7, at time  $T_p$  the preamble's first symbol 757 has fully arrived and the preamble's second symbol 758 is currently emerging. The contents of the shift register at time  $T_p$  correspond to the contents of window 782 seen in the lower comparator output sample stream 707. The window 782 effectively moves to the right after time  $T_p$  as new samples are entered into the

register 1004 input (on the right as seen in Figure 10) and the oldest, leftmost sample is expired.

Referring back to Figure 9, it is important to note that a sample delay unit 902, 903, 904 may be formed with approaches other than a shift register. For example, a first in first out (FIFO) queue may be used that builds up the state of the queue to N samples before removing the oldest sample from the queue. After building up the queue state to N samples, the oldest sample is serviced from the queue as each new sample is added. This keeps the queue state at N samples. Samples shift closer to the exit of the queue with each newly added sample.

As another embodiment, samples may be stored in a memory (e.g., a DRAM or SRAM chip external to the semiconductor chip having the slicer or embedded DRAM or SRAM space on the semiconductor chip having the slicer). The memory may be used to support other functions in the receiving device such as digital signal processor (DSP), microprocessor or filter. Rather than shifting older samples with each new sample, the circuitry used to control the memory addressing can be configured to rotate with modulo N such that the oldest sample in memory is continually overwritten.

Referring to Figures 6, 8 and 9, in light of the discussion of the slicer's operation provided above with respect to Figure 8, recall that the offset sensing unit 660, 960: 1) determines the mode used by the offset compensation loop 611 in light of the accuracy of the threshold level (and/or the occurrence of a significant event such as the recognition of a packet's preamble); and 2) analyzes the comparator tree 601 output samples 705, 706, 707 in search of the packet's preamble 790. Both of these operations are discussed immediately below.

Referring to the offset sensing unit 960 of Figure 9, note the presence of correlation units 912, 913, 914 respectively coupled to each sample delay unit 902, 903, 904. A correlation is a mathematical technique that may be used to compare the similarity of two data patterns. To perform a correlation, typically, a first data pattern is convoluted with a second data pattern.

The result of the correlation is a "spike", the height of which provides a measurement of the degree of similarity between the two data patterns. That is, the more similar the pair of correlated data patterns (as to their shapes, features, etc.), the higher the height of the spike becomes. Thus, if a pair of identical data patterns are correlated, the spike resulting from their convolution has a maximum height. If the pair of completely dissimilar data patterns are correlated, the spike has no height (i.e., does not exist). More information regarding correlation may be found in a U.S. Patent entitled Method and Apparatus for Identifying a Pre-Determined Pattern from a Received Signal Via Correlation filed on September 27, 2000.

The collection of samples in each sample delay unit 902, 903, 904 may be viewed as a data pattern. Each of these data patterns are correlated with a previously stored data pattern by their respective correlation unit. Thus, the data pattern held in sample delay unit 902 is correlated against a previously stored data pattern by correlation unit 912, the data pattern held in sample delay unit 903 is correlated against a previously stored data pattern by correlation unit 913, the data pattern held in sample delay unit 904 is correlated against a previously stored data pattern by correlation unit 914.

The previously stored data patterns may be supplied (directly or indirectly) by a read only memory 921 (ROM) and stored in registers 915, 916, 917 that are respectively coupled to a correlation unit 912, 913, 914 (as shown in Figure 9). Registers 915, 916, 917 allow for quick access of the previously stored data patterns by the correlation units 912, 913, 914.

The slicer effectively "looks for" particular comparator output sample stream patterns by correlating the previously stored data patterns with the contents of the sample delay units 902, 903, 904. In an embodiment, correlations are performed for each position of the sliding window (i.e., separate correlations are performed after each new comparator output sample). Thus, each correlation unit 912, 913, 914 continually "checks" the most recent collection of comparator output samples to see if they "match" a predetermined "looked for" pattern.

In an embodiment, during preamble acquisition mode, the correlation units 902, 903, 904 continually correlate comparator output samples against a pre-determined data pattern in search of comparator output sample patterns that indicate either the need to place the slicer in fast attack mode or the fact that the preamble has arrived. This is achieved by correlating comparator output samples against a first pre determined data pattern (to understand if fast attack mode is needed) and a second pre determined data pattern (to understand if the preamble is arrived). Note that if the baseband signal has a small offset (i.e., within TH1 and TH2), the fast attack mode is simply not entered.

Note that registers 915, 916, 917, as drawn in Figure 9, should have space available for both patterns. That is, for example, register 915 is partitioned into two sections 918, 919. Section 918 may be used to store the first pattern while section 919 may be used to store the second pattern. Registers 916 and 917 are similarly partitioned into spaces 920, 921 and 922, 923.

Referring to region 783 of the comparator samples 705, 706, 707 in Figure 7 (i.e., just after the baseband signal changes its offset at time Tx), note that the values of the samples are equal in value once the sampled and held signal 751 falls below the lower threshold TH2. That is, just after time Tx, the sampled and held signal 751 falls below all three thresholds TH1, TH3 and TH2. This causes each of the comparators 602, 603, 604 to produce an output value of "0" as seen in signals 702, 703, 704.

Entry into Fast Attack mode may be triggered upon comparing the output signals 702, 703, 704 or samples 705, 706, 707. Specifically, if signals 702 and 704 or samples 705 and 707 are equal, the offset 556b is outside TH1 and TH2. These comparisons may be enhanced by the use of correlation techniques as discussed in the embodiments that follow.

If the correlation units 912, 913, 914, continually correlate the contents of the sample delay units 902, 903, 904 with a previously stored data pattern (located in registers, 915, 916, 917) that correspond to a string of 0s (e.g., 00000000), the height of the correlation "spike" produced at the Fast\_Attack\_Down correlation unit

outputs 967, 968, 969 becomes larger as the samples of region 783 begin to accumulate in the sample delay units 902, 903, 904. The correlation units 912, 913, 914 may be designed to trigger a "match", signifying the looked for data pattern has been found, when the correlation "spike" reaches or surpasses a specific height. The specific height may vary from embodiment to embodiment depending on the density of samples, the size of the grace period  $T_g$ , etc.

As an example, assume that a previously stored eight bit pattern, 00000000, is correlated by each correlation unit 912, 913, 914 against the contents of its corresponding sample delay unit 902, 903, 904. The height of the FAST ATTACK correlation spikes from each correlation unit 912, 913, 914 will be a maximum at time  $T_{y1}$  of Figure 7 because, as of time  $T_{y1}$ , eight consecutive 0s will be located in each 902, 903, 904 sample delay unit.

If the threshold for triggering a match is the maximum spike height (e.g.,  $X$  as thresholded by comparison units 910a,b,c), all three correlation units will simultaneously trigger a match after the correlation performed at time  $T_{y1}$  in Figure 7. When each Fast\_Attack\_Down output 967, 968, 969 simultaneously indicates a match at time  $T_{y1}$ , a fast attack mode bit 749 is set, which (referring briefly to Figure 6) is communicated to the offset compensation loop 611. This activity acts as a comparison of the sample stream valves 705, 706, 707.

As the baseband signal 751 rises above the lower threshold level TH2 after time  $T_{y1}$ , the correlation spike from the lower correlation unit 914 will begin to fall because logic 1s begin to enter its sample and hold unit 904. The falling correlation spike causes the Fast\_Attack\_Down output 969 to drop which consequently drops the FA\_DOWN bit 749 from the AND gate 977. This causes the slicer's offset compensation loop to re-enter the preamble acquisition mode as discussed with respect to Figure 8.

Before continuing with a discussion of the correlation used to detect the preamble, a few points are worth mentioning regarding the entry/de-entry to/from fast attack mode discussed just above. First, note that if the baseband signal 755 were to have an offset polarity opposite that shown in Figure 7 (i.e.,

such that the baseband signal rises above the TH1 threshold rather than below the TH2 threshold level), region 783 would comprise "1"s rather than "0s".

Thus, the first data pattern described above used to detect whether or not fast attack mode is needed may actually be implemented with two data patterns: one being a consecutive string of 0s (to detect demodulator signals below TH2) and one being a consecutive string of 1s (to detect demodulator signals above TH1). These may be correlated in series or in parallel with one another.

Consistent with this approach, note that two "fast attack" outputs are utilized. The first Fast\_Attack\_Down outputs 967, 968, 969, as discussed above, signify that the baseband signal is below all three threshold levels TH1, TH3, TH2. The set of Fast\_Attack\_Up outputs (which correlate against a string of consecutive 1s) signify that the baseband signal is above all three threshold levels TH1, TH3, TH2. As a result two fast attack mode bits are formed at the output of the offset sensing unit 960: FA\_UP and FA\_DOWN. If the FA\_UP bit is high, the threshold levels will be moved up by the offset compensation loop. If the FA\_DOWN bit is high the threshold levels will be moved down by the offset compensation loop.

Furthermore, if the demodulator exhibits less than perfect channel isolation, it is possible that the low power (i.e., small amplitude) baseband signals from channels other than the channel to be received will be presented to the slicer. Signals may be deemed "qualified" for further processing if they have an amplitude outside the outer thresholds (i.e., above TH1 and below TH3). This acts akin to a signal detect that ignores the weaker, low amplitude signals from an incorrect channel.

Also, note that based on the spacing Y between the threshold levels (in light of the amplitude of the preamble signal), temporal regions 784, 785, 786 and 787 of simultaneously equal comparator output signal samples appear near/at the peaks 788, 789, 790, 791 of the preamble. Note however, these regions have a smaller width W2 than the width W1 of the region 783 that triggered the fast attack mode.

If W1 and W2 were equal in width, the slicer could mistakenly "misidentify" the peaks 788, 789, 790, 791 of the preamble as a need for entry to the

fast attack mode. That is, the "fast attack match" outputs 967, 968, 969 would simultaneously indicate a match (setting the fast attack mode bit high) for each peak 788, 789, 790, 791 of the preamble because the same number of consecutive, equal logic values would exist in region 783 as in regions 784, 785, 786 and 787.

However, as W1 is made greater than W2 (i.e., as more consecutive, equal logic values are looked for in order to trigger the fast attack mode), the height of the correlation spikes produced in regions 784, 785, 786, 787 fall below the height of the spike produced by the correlations in region 783. That is, as less consecutive, equal values exist in regions 784, 785, 786, 787 they do not significantly resemble the looked for pattern. Better said, the looked for pattern in the example of Figure 7 has eight consecutive equal values while the preamble is only capable of producing five.

The difference in correlation spike height as between region 783 and regions 784, 785, 786, 787 may be used to prevent the slicer's entry into fast attack mode during the reception of the preamble. That is, the higher the spike height associated with region 783 is sufficient to set the "fast attack match" outputs 967, 968, 969 while the lower spike height associated with regions 784, 785, 786, 787 are not.

Note that the width W2 of regions 784, 785, 786, 787 may be controlled by designing for a certain preamble amplitude against specific TH1 and TH2 levels. That is, as the TH1 level moves closer to the maximum preamble peak and the TH2 level moves closer to the minimum preamble peak, the width W2 of regions 784, 785, 786 and 787 becomes smaller. At an extreme, they may be designed such that TH1 is above the maximum preamble peak and TH2 is below the maximum preamble peak.

In this case, W2 is zero (i.e., regions 784, 785, 786 and 787 do not exist). This allows for a minimal usable width W1 for region 783. That is, the correlation spike height used to "catch" the need for the fast attack mode may be minimal because no spike is produced at the preamble peaks. Note that a smaller region 783 width

W2 corresponds to the slicer's ability to identify the need for fast attack mode sooner. That is, time  $T_{y1}$  moves closer to time  $T_x$  as W2 shortens.

Workable ranges of W2 and W1 bring forth a tradeoff between the fast attack mode offset compensation loop bandwidth and the preamble acquisition mode offset compensation loop bandwidth. As W2 is reduced, the slicer can identify the need for the fast attack mode sooner (i.e.,  $T_{y1}$  is closer to time  $T_x$ ). This allows for a lower fast attack mode offset control loop bandwidth because for a given grace period  $T_g$ , the fast attack mode has more time to correct for the threshold error.

However, reducing W2 creates the need for an even smaller W1 (so that the fast attack mode is not inadvertently triggered during the arrival of the preamble). Reduced W1 may be produced by moving the threshold levels TH1, TH2 farther away from TH3 (i.e., increasing their spacing Y). Having increased threshold spacing Y means the slicer can re-enter preamble acquisition mode with a greater remaining threshold error.

That is, since the slicer re-enters the preamble acquisition mode when TH1 rises above the baseband signal falls or TH2 falls below the demodulator signal, this leaves a remaining threshold error approximately equal to Y for the offset compensation loop to correct for. In order to correct for the remaining threshold error (Y) before the preamble arrives, larger offset compensation loop bandwidths may be used during preamble acquisition mode for slicers designed with a large Y as compared to the offset compensation loop bandwidths that may be used during preamble acquisition mode for slicers designed with a small Y.

Note that as an alternative embodiment, rather than storing a predetermined fast attack mode pattern in a register (as described above) and correlating it against the comparator output signal samples, the contents of the sample delay units may be correlated with one another. When the samples are equal, as in region 783, a large correlation spike will be produced. Thus, rather than sending the contents of each sample delay line unit 902, 903, 904 to its own

correlation unit 912, 913, 914, they may alternatively be delivered to a single correlation unit capable of performing a correlation between three sets of samples.

Correlation units 902, 903, 904 may be formed by hardwired logic (such as within an application specific integrated circuit (ASIC) or standard product offering), programmable logic (as within an field programmable gate array (FPGA) or other programmable technology) or by a digital signal processor or microprocessor that executes software configured to execute the methodology described above.

Detection of the preamble may be made by methods similar to those described above. That is, a predetermined pattern of samples (that resemble the samples that should appear in the sample delay units when the preamble arrives) is stored in a register and correlated against the sample delay unit's samples. In an embodiment, the sample delay units are four symbols wide so that the entire preamble can be stored in the sample delay units when it arrives. Exemplary predetermined patterns 795, 796, 797 for this approach are shown in Figure 7 (using the sample streams 705, 706, 707 for simplicity) for each of the three correlation units 912, 913, 914 respectively.

Note that, by design, the predetermined patterns 795, 796, 797 match the received data samples of Figure 7. The height of the correlation spikes correlated against these patterns 795, 796, 797 will reach a maximum when the preamble is fully stored in the sample delay units 902, 903, 904. This will trigger a logic high at the "preamble detect" outputs 991, 992, 993 of the correlation units 912, 914, 913. Note that noise or other "bit flips", as well as some error in the threshold level should be accounted for when determining the acceptable correlation spike height for preamble detection.

For example, notice that the looked for sample pattern 786 from the central comparator sample stream 706 has a 50-50 duty cycle. In reality, the central threshold level TH3 may not be perfect when the preamble arrives - resulting in a duty cycle other than 50-50 in the samples collected by the central sample delay unit 902. The effect will be a lower correlation spike height for the preamble's

samples (as compared to a perfectly thresholded preamble). Thus, some margin for lower, acceptable spike heights may be designed into the correlation units 912, 913, 914.

Note that the predefined data patterns utilized by each correlation unit during their search for the preamble have different duty cycles because of the different thresholds used by each comparator. Those of ordinary skill will be able to determine the appropriate oversampling rates, correlation spike heights, etc. that are acceptable for a desired amount of threshold error, duty cycle distortion, etc.

Figure 11 shows an embodiment 1111 for the offset compensation loop 611 of Figure 6. Recall that the offset compensation loop 611 effectively averages the baseband signal 650 to produce a threshold against which the baseband signal may be sliced. Also recall that the offset compensation loop operates at different bandwidths depending on the appropriate slicer mode as determined by the offset sensing unit 660.

Specifically, the slicer embodiment of Figure 11 has three operative modes: 1) a fast attack mode; 2) a preamble acquisition mode; and 3) a tracking mode. Under the fast attack mode, the offset compensation loop operates at its highest bandwidth. Under the tracking mode, the offset compensation loop operates at its lowest bandwidth. Under the preamble acquisition mode, the offset compensation loop operates at a bandwidth between its highest and lowest bandwidths.

In the offset compensation loop embodiment of Figure 1111, the Fast Attack\_UP, Fast Attack\_DOWN and Preamble Detect input lines are the Fast Attack\_UP, Fast Attack\_DOWN and Preamble Detect output lines associated with the offset sensing unit 960 of Figure 9. Control chart 1101 of Figure 11 indicates how the input bits are used to control the mode of the offset compensation loop. Operational characteristics used by all the modes are discussed first, followed by a discussion of the operational characteristic unique to each mode.

The offset compensation loop embodiment of Figure 11 includes an accumulator 1104, a scaling unit 1105 and a digital to analog (D/A) converter 1106.

The offset compensation loop 1111 is designed from the perspective of an error term. In the embodiment of Figure 11, the error term is a digital word (i.e., a plurality of bits) that is presented to the input of the accumulator 1104.

The error term has two components: a polarity and a value. For a particular threshold adjustment, the polarity of the error term controls the direction of the adjustment (i.e., up or down) while the value of the error term controls the amount of the adjustment (i.e., how many volts the threshold is adjusted). Because a higher loop bandwidth corresponds to faster threshold adjustments (i.e., greater adjustment per unit of time) as compared to a lower loop bandwidth, the bandwidth of the offset compensation loop 1111 is controlled by controlling the magnitude of the error term value.

Thus, the fast attack mode employs large error term values so that large adjustments are made to the threshold per unit time. Similarly, the tracking mode employs small error term values so that small threshold adjustments are made per unit of time. The preamble acquisition mode employs error term magnitudes in between the large and small magnitudes associated with the other two modes so that medium adjustments are made to the threshold per unit of time.

A series of individual error terms are clocked sequentially into the accumulator 1103. The accumulator "accumulates" the individual error terms which, over time, add up to a value that corresponds to the proper adjustment. An accumulator 1103 may be formed as shown in Figure 11 with an adder 1108 having its output node coupled to a storage element 1109 (e.g., a register or flip-flop capable of holding the adder 1108 output word) where the storage element is coupled (via a feedback arrangement) to one of the accumulator input nodes 1110.

In order to produce a new accumulator output value (which corresponds to a new adjustment to be made to the threshold level), the accumulator 1103 adds its current output value to a new error term. That is (in the embodiment of Figure 11) when a new error term is presented to the adder 1108, the adder 1108 presents the storage element 1109 with the summation of the accumulator's current output value and the new error term. This summation is then clocked into the storage

element 1109 to produce a new accumulator output value. New accumulator output values can therefore be presented at the rate of the clock coupled to the storage element.

The accumulator output value may then be scaled again (at the designer's option) with a scaling unit 1104. The scaling unit 1105 multiplies the value of the accumulator output word by a constant. The output word of the scaling unit 1105 (if used) or the output word of the accumulator 1103 is then applied to a digital to analog converter 1106. The digital to analog converter 1106 converts the value of the digital word presented at its input into a corresponding DC voltage at its output. This voltage is then applied to the input of the comparator tree (at threshold level TH3) as shown back in Figure 6.

Recall from above that the error term controls the size and direction of a threshold adjustment. Error term unit 1112 is responsible for determining the error term. This error term unit 1112 may be viewed as being partitioned into two regions 1113, 1114. A first region 1113 determines the error term when the slicer is in fast attack mode. A second region 1114 determines the error term when the slicer is not in fast attack mode.

The output of the active region 1113, 1114 (i.e., region 1113 if the slicer is in fast attack mode or region 1114 if the slicer is not in fast attack mode) is presented to the accumulator by multiplexer 1115. The channel select input 1116 of the multiplexer 1115 is controlled, in the embodiment of Figure 11, by the state of the fast attack mode inputs 1116, 1117. If either of the fast attack mode inputs 1116, 1117 are a logic high (signifying the slicer is to be placed in fast attack mode), the multiplexer 1115 enables the output of region 1113.

Region 1113 (the fast attack region) creates an error term having a fixed value ("Z"). The polarity of the error term is based upon the direction the threshold needs to be adjusted. Presenting a negative value to the accumulator input will lower the accumulator output value (which consequently lowers the threshold). Similarly, presenting a positive value to the accumulator input will raise the accumulator output value (which consequently raises the threshold).

The channel select input 1120 of the multiplexer is configured to enable the proper polarity error term in light of the fast attack mode inputs. Thus, if the threshold needs to be lowered (as indicated by a logic low on the fast attack mode\_UP input 1117) an error term of  $-Z$  is forwarded to multiplexer 1115. Similarly, if the threshold needs to be raised (as indicated by a logic high on the fast attack mode\_UP input 1117) an error term of  $+Z$  is forwarded to multiplexer 1115.

Note that  $Z$  can be implemented as a digital word of  $n$  bits. In order to ensure that the fast attack mode has a higher bandwidth than the other modes, the value of  $Z$  may be configured to be equal to or greater than the maximum possible error term from region 1114 (although note that this is not an absolute requirement). Because the value of  $Z$  is fixed, the series of error terms produced by error term unit 1112, while the slicer is in fast attack mode, will also be fixed.

As a consequence, the adjustments made by the offset compensation loop to the threshold are the same. Recall this feature was originally shown and discussed in Figure 7. That is after time  $T_{y1}$  in Figure 7, when the slicer operates in fast attack mode, note the fixed series of adjustments made to the threshold. Applying a series of large, fixed error terms when in fast attack mode input allows the slicer to have a stable, high bandwidth offset compensation loop (i.e., the large overshoot and long settle time associated with higher bandwidth loops is avoided).

When the slicer is not in fast attack mode, it is either searching for the preamble with a moderate loop bandwidth or, having found the preamble, is actively tracking the baseband signal symbols that follow the preamble with a low loop bandwidth. Region 1114 determines the error term in either of these modes. The different loop bandwidths are controlled by adjusting the scaling of a subtractor 1122 output as discussed in more detail below.

The subtractor 1122 takes the difference between two values. The first value is 0.500. The second value is the average over a previous number of center comparator output samples. That is, a sample delay unit 1123 (similar to the sample delay unit 903 of Figure 9) collects the most recent number of center delay

samples (up to a certain amount) to effectively form a sliding window as discussed with respect to Figures 7 and 9.

The samples in the sample delay unit 1123 are averaged by averaging logic 1124. Note that the contents of the sample delay unit 1123 are binary (i.e., a "1" or a "0"). Thus the average produced by averaging unit 1123 ranges between a maximum of 1.000 (when the sample delay unit 1123 contains only 1s) and a minimum of 0.000 (when the sample delay unit 1124 contains only 0s). The average obtained by the averaging unit 1124 is then presented to the subtractor 1122.

The subtractor 1122 subtracts 0.500 from the output of the averaging unit 1124. The subtractor 1122 produces a preliminary error term (e.g., as just a few examples: -0.500 for an average of 0.000; -0.250 for an average of 0.250; 0.000 for an average of 0.500, 0.250 for an average of 0.750, and 0.500 for an average of 1.000) having a polarity and magnitude indicative of the adjustment that should be made to the present threshold level.

If the polarity of the subtractor 1122 output is negative, the output of the averaging unit 1124 is less than 0.500 (because more than half the samples are a logic 0) which indicates the current threshold level is above the average value of the baseband signal. In this case, the threshold should be lowered. Adding the negative subtractor output (or a scaled version of it) to the current accumulator value will properly lower the value of the current threshold level.

Similarly, if the polarity of the subtractor 1122 output is positive, the output of the averaging unit 1124 is greater than 0.500 (because more than half the samples are a logic 1) which indicates the current threshold level is below the average value of the baseband signal. In this case, the threshold should be raised. Adding the positive subtractor output (or a scaled version of it) to the current accumulator value will properly raise the value of the current threshold level.

A larger subtractor unit output magnitude indicates the threshold is farther away from the baseband signal average than a smaller subtractor unit output. That is, a threshold level that produces an averaging unit 1124 output value of + or

- 0.750 is farther away from the baseband signal offset than a threshold level that produces an average output value of + or - 0.250.

The magnitude of the change made to the accumulator output is related to the magnitude of the subtractor 1122 output. That is, a large subtractor 1122 output magnitude value produces a greater change to the accumulator output value (which consequently produces a larger threshold adjustment) than a small subtractor output magnitude. Thus, for example, a subtractor 1122 output value of 0.750 will produce a greater adjustment to the threshold than a subtractor 1122 output value of 0.250.

These principles of design are inherently stable. That is, the threshold level is raised/lowered as its position falls below/above the baseband signal average; and, furthermore, the amount the threshold is adjusted increases/decreases as the threshold becomes farther from/closer to the baseband signal average. As a natural result of this stability, the threshold continually approaches and eventually settles to a level that produces an averaging unit 1124 output of 0.500. Because an averaging unit 1124 output of 0.500 corresponds to the threshold being placed at the baseband signal offset, the threshold settles at the demodulator signal offset.

This is seen in Figure 7 during the slicer's preamble acquisition mode operation prior to time Tx (when the transmitting device's carrier arrives) and after time Ty2 when the slicer exits fast attack mode. Prior to time Tx, the slicer has already stabilized at the baseband signal average. As a result, the central comparator randomly "chatters" from the baseband signal noise. The random noise produces approximately equal numbers of 1s and 0s which corresponds to an average value of 0.500.

After time Ty2, the slicer re-enters the preamble acquisition mode. Referring to Figure 11, note that the entry of the slicer into fast attack mode causes the sample delay unit 1123 to "clear" (i.e., empty its contents). Thus, at time Ty2 when the slicer re-enters preamble acquisition mode, the sample delay unit 1123 begins to accumulate fresh central comparator samples.

Because the central threshold level TH3 is still above the baseband signal at time  $T_{y2}$ , the sample delay unit 1123 immediately begins to accumulate samples having a value of "0" which results in an average value of 0.000. This produces a negative term at the subtractor 1122 output which further lowers the central threshold TH3 as seen in Figure 7. The central threshold TH3 eventually settles to the baseband signal offset.

The preamble acquisition mode's loop bandwidth is a function of scaling unit 1125 and the depth of the sample delay unit 1123 (i.e., how many samples the scaling unit holds). Generally, the loop bandwidth increases as the scaling unit  $k_1$  increases and the sample delay unit 1123 depth decreases. Scaling unit 1125 effectively multiplies the preliminary output term from the subtractor 1122 by a constant  $k_1$ .

Thus, for a given subtractor 1122 output value magnitude, a larger  $k_1$  presents a larger magnitude input to the accumulator (causing a larger adjustment to the threshold level) than a smaller  $k_1$ . Similarly, a smaller sample delay unit 1123 depth allows the subtractor output to reflect sudden changes in the position of the baseband signal (with respect to the threshold level TH3) because each sample has a greater weight in the average that is calculated by the averaging unit 1124.

If the preamble has not been found, as discussed above, the slicer will be in preamble acquisition mode (unless it is in fast attack mode). The preamble detect input 1118 (provided by the offset compensation loop unit) indicates whether or not the preamble has been found and may therefore be used to control the loop bandwidth. As seen in Figure 11, if the preamble found input 1118 is low (indicating the preamble has not been found), the scaling unit 1125 has a scaling factor of  $k_1$ . Alternatively (or in combination) a first sample delay unit 1123 depth may also be established.

After the preamble is found, the preamble detect input 1118 goes high and the slicer enters tracking mode. The scaling unit 1125 is adjusted to have a lower scaling  $k_2$  (where  $k_1 > k_2$ ) as a result. Because  $k_2$  is less than  $k_1$ , the magnitude of

the error terms presented to the accumulator 1103 (for an identical subtractor 1122 output value) will be lower when the preamble is found. This corresponds to a lower loop bandwidth. Alternatively, or in combination, the depth of the sample delay unit 1123 may be increased as compared to the depth employed during the preamble acquisition mode.

Note that sample delay unit 1123 may be a separate sample delay unit from the sample delay unit 903 of Figure 9 (which also collects samples from the central comparator's output signal). Alternatively, sample delay unit 1123 used in the offset compensation loop 1111 may be the same sample delay unit 902 employed in the offset sensing unit. The front portion(s) of sample delay unit 902 may be used (rather than its entire contents) for sample delay unit 1123 if the depth of sample delay unit 1123 is to be less than the depth of sample delay unit 903.

As an alternative embodiment, the sample delay unit 1123 and averaging unit 1124 may be disposed of. That is, the samples from the center comparator may be fed directly into the subtractor 1122. This approach is also inherently stable. That is, the central threshold level TH3 will approach and eventually settle to the average of the baseband signal.

Referring to Figure 6, note that other offset sensing approaches may be configured to observe the output signals from a comparator tree arrangement and/or other offset compensation loop approaches may be configured to adjust the threshold level of a comparator tree arrangement, besides those discussed above. Once the pre-determined pattern (e.g., preamble) is discovered, the central comparator 602 output signal will provide a correct interpretation of the baseband signal (similar to that seen in Figure 3a). As such the center comparator 602 output signal may be forward to downstream circuitry as the slicer output.

It is important to point out that the discussion above is applicable to other applications besides preamble detection for a BLUETOOTH device. The teachings above may be applied to any receiver desiring to identify a particular data sequence (i.e., a predetermined pattern). That is, sequences other than a 1010

preamble (e.g., such as a synchronization word within a BLUETOOTH packet) may be found by techniques similar to those described above.

Furthermore, it is also important to note that the present teachings may be used to detect any predetermined pattern from a signal having a sudden offset. Thus, the present teachings are also applicable to other frequency shift keyed wireless technologies besides BLUETOOTH such, as just a few examples, HomeRF, IEEE 802.11, GSM and Digitally Enhanced Cordless Telephony (DECT).

Embodiments of the above discussion may be manufactured as part of a semiconductor chip (e.g., by a planar semiconductor manufacturing process). Note also that embodiments of the present description may be implemented not only as part of a semiconductor chip but also within machine readable media. For example, the designs discussed above may be stored upon and/or embedded within machine readable media associated with a design tool used for designing semiconductor devices. Examples include a netlist formatted in the VHSIC Hardware Description Language (VHDL) language, Verilog language or SPICE language. Some netlist examples include: a behavioral level netlist, a register transfer level (RTL) netlist, a gate level netlist and a transistor level netlist. Machine readable media also include media having layout information such as a GDS-II file. Furthermore, netlist files or other machine readable media for semiconductor chip design may be used in a simulation environment to perform the methods of the teachings described above.

Thus, it is also to be understood that embodiments of this invention may be used as or to support a software program executed upon some form of processing core (such as the CPU of a computer) or otherwise implemented or realized upon or within a machine readable medium. A machine readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical

or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

**CLAIMS**

What is claimed is:

1. An apparatus, comprising:
  - a) a first comparator having a first input that receives a first threshold and a second input that receives an input signal;
  - b) a second comparator having a first input that receives a second threshold, said second threshold less than said first threshold, said second comparator having a second input that receives said input signal; and
  - c) an offset sensing unit that detects said input signal above said first threshold or below said second threshold by comparing said first and second comparator outputs.
2. The apparatus of claim 1 further comprising a third comparator having a first input that receives a third threshold, said third threshold between said first threshold and said second threshold, said third comparator having a second input that receives said input signal.
3. The apparatus of claim 2 wherein said third threshold is a primary threshold.
4. The apparatus of claim 2 wherein said third threshold is midway between said first threshold and said second threshold.
5. The apparatus of claim 1 further comprising an offset compensation loop unit that positions said first threshold above an offset of said input signal and positions said second threshold below said offset of said input signal by presenting a sequence of error terms to an accumulator in response to said detection.
6. The apparatus of claim 5 wherein said error terms have the same magnitude.
7. The apparatus of claim 5 wherein said detection is communicated from said offset detection unit to said offset compensation loop unit by either of a pair

of signals, a first of said signals indicative of said input signal being above said first threshold, a second of said signals indicative of said input signal being below said second threshold.

8. The apparatus of claim 1 further comprising a sample delay unit input coupled to an output of said first comparator.
9. The apparatus of claim 8 further comprising a correlation unit coupled to an output of said sample delay unit.
10. The apparatus of claim 9 further comprising a register that holds a predetermined data pattern, said register coupled to said correlation unit.
11. The apparatus of claim 1 further comprising a demodulator output coupled to said second inputs of said comparators.
12. The apparatus of claim 11 further comprising a sample and hold circuit between said demodulator and said second inputs of said comparators.
13. An apparatus, comprising:
  - a) a first comparator having a first input that receives a first threshold and a second input that receives an input signal;
  - b) a second comparator having a first input that receives a second threshold, said second threshold less than said first threshold, said second comparator having a second input that receives said input signal;
  - c) a third comparator having a first input that receives a third threshold, said third threshold between said first threshold and said second threshold, said third comparator having a second input that receives said input signal; and
  - d) an offset sensing unit that detects said input signal above said first threshold or below said second threshold by comparing said first and second comparator outputs.
14. The apparatus of claim 13 wherein said third threshold is a primary threshold.

15. The apparatus of claim 14 wherein said third threshold is midway between said first threshold and said second threshold.
16. The apparatus of claim 13 further comprising an offset compensation loop unit that positions said first threshold above an offset of said input signal and positions said second threshold below said offset of said input signal by presenting a sequence of error terms to an accumulator in response to said detection.
17. The apparatus of claim 16 wherein said error terms have the same magnitude.
18. The apparatus of claim 16 wherein said detection is communicated from said offset detection unit to said offset compensation loop unit by either of a pair of signals, a first of said signals indicative of said input signal being above said first threshold, a second of said signals indicative of said input signal being below said second threshold.
19. The apparatus of claim 16 wherein said offset compensation loop unit further comprises a first bandwidth and a second bandwidth, said first bandwidth greater than said second bandwidth, said offset compensation loop unit employing said first bandwidth if said detection occurs, said offset compensation loop unit employing said second bandwidth if said detection does not occur.
20. The apparatus of claim 19 wherein said offset compensation loop unit further positions, when employing said second bandwidth, said third threshold at said input signal offset by taking the difference between said third comparator output signal and 0.5 to generate a second sequence of error terms.
21. The apparatus of claim 20 wherein said second sequence of error terms have magnitudes less than the magnitude of said sequence of error terms.
22. The apparatus of claim 19 wherein said offset compensation loop unit further positions, when employing said second bandwidth, said third threshold at

said input signal offset by taking the difference between the average of said third comparator output signal and 0.5 to generate a second sequence of error terms.

23. The apparatus of claim 22 wherein said second sequence of error terms have magnitudes less than the magnitude of said sequence of error terms.
24. The apparatus of claim 16 wherein said offset compensation loop unit further comprises a third bandwidth, said third bandwidth less than said second bandwidth, said offset compensation loop unit employing said third bandwidth after a preamble is detected.
25. The apparatus of claim 13 further comprising a sample delay unit input coupled to an output of said third comparator.
26. The apparatus of claim 25 further comprising a correlation unit coupled to an output of said sample delay unit.
27. The apparatus of claim 26 further comprising a register that holds a predetermined data pattern, said register coupled to said correlation unit.
28. The apparatus of claim 27 wherein said predetermined data pattern corresponds to a preamble for a BLUETOOTH packet.
29. The apparatus of claim 13 further comprising a demodulator output coupled to said second inputs of said comparators.
30. The apparatus of claim 29 further comprising a sample and hold circuit between said demodulator and said second inputs of said comparators.
31. The apparatus of claim 13 wherein said offset detection unit detects said input signal above said first threshold or below said second threshold by comparing said first, second and third comparator outputs.
32. A method, comprising:
  - a) comparing an input signal against a first threshold and a second threshold to generate a first thresholded signal and a second thresholded signal, said first threshold higher than said second threshold; and

- b) detecting if said input signal is above said first threshold or below said second threshold by comparing said first and second thresholded signals.
33. The method of claim 32 wherein said detection is triggered if said first and second thresholded signals are equal.
34. The method of claim 33 wherein a signal indicative that said input signal is above said first threshold is generated if said first and second threshold signals are equal to 1.
35. The method of claim 33 wherein a signal indicative that said input signal is below said second threshold is generated if said first and second threshold signals are equal to 0.
36. The method of claim 32 further comprising storing samples of said first thresholded signal into a sample delay unit.
37. The method of claim 36 further comprising correlating said samples against a pre-determined pattern.
38. The method of claim 37 wherein said pre-determined pattern is a sequence of 0s.
39. The method of claim 37 wherein said pre-determined pattern is a sequence of 1s.
40. The method of claim 39 wherein the length of said sequence of 1s is greater than the length of a second sequence of 1s found in said first thresholded signal when said input signal has a symbol peak above said first threshold.
41. The method of claim 32 further comprising sending a signal to an offset compensation loop unit if said detection arises, said signal indicative of whether said input signal is above said first threshold or below said second threshold, said offset compensation loop unit having an output that controls said first and second thresholds.
42. The method of claim 41 further comprising generating a series of error terms in response to said signal.

43. The method of claim 42 wherein said error terms are added to adjust said offset compensation loop unit output.
44. The method of claim 41 further comprising comparing said input against a third threshold to generate a third thresholded signal, said third threshold between said first and second thresholds.
45. The method of claim 44 further comprising storing samples of said third thresholded signal into a sample delay unit.
46. The method of claim 45 further comprising correlating said samples against a pre-determined pattern.
47. The method of claim 47 wherein said pre-determined pattern corresponds to a BLUETOOTH packet preamble.
48. The method of claim 44 further comprising sending a second signal to said offset compensation loop unit indicative of whether a preamble within a packet has been found.
49. The method of claim 48 further comprising adjusting said first, second and third thresholds with a higher bandwidth if said signal is active and adjusting said first, second and third thresholds with a lower bandwidth if said signal is not active.
50. The method of claim 49 further comprising adjusting said first, second and third thresholds according to a first lower bandwidth if said preamble has not been found and a second lower bandwidth if said preamble has been found, said first lower bandwidth greater than said second lower bandwidth.
51. A method, comprising:
- a) adjusting a first, second and third thresholds with a feedback loop, said feedback loop having a first bandwidth if a signal is above said first threshold or below said second threshold, said third threshold below said first threshold and above said second threshold; and
  - b) adjusting said first, second and third thresholds with said feedback loop, said feedback loop having a second bandwidth if said signal is between said

first and second thresholds, said first bandwidth greater than said second bandwidth.

52. The method of claim 51 wherein said adjusting further comprises adding a sequence of error terms within said feedback loop to change an output level of said feedback loop.

53. The method of claim 52 further comprising converting said feedback loop output level from a digital representation to an analog voltage before applying said adjustment.

54. The method of claim 51 wherein each of said error terms further comprise a magnitude indicative of said adjusting amount.

55. The method of claim 54 wherein said error term magnitudes are greater when said feedback loop operates in said first bandwidth than when said feedback loop operates in said second bandwidth.

56. The method of claim 54 wherein said error term magnitudes are the same when said feedback loop operates in said first bandwidth.

57. The method of claim 54 wherein said second bandwidth further comprises a higher second bandwidth and a lower second bandwidth, said higher second bandwidth employed if a packet's pre-determined data pattern has not been found, said lower second bandwidth employed if said packet's pre-determined data pattern has been found.

58. The method of claim 57 wherein said packet's pre-determined data pattern is a BLUETOOTH preamble.

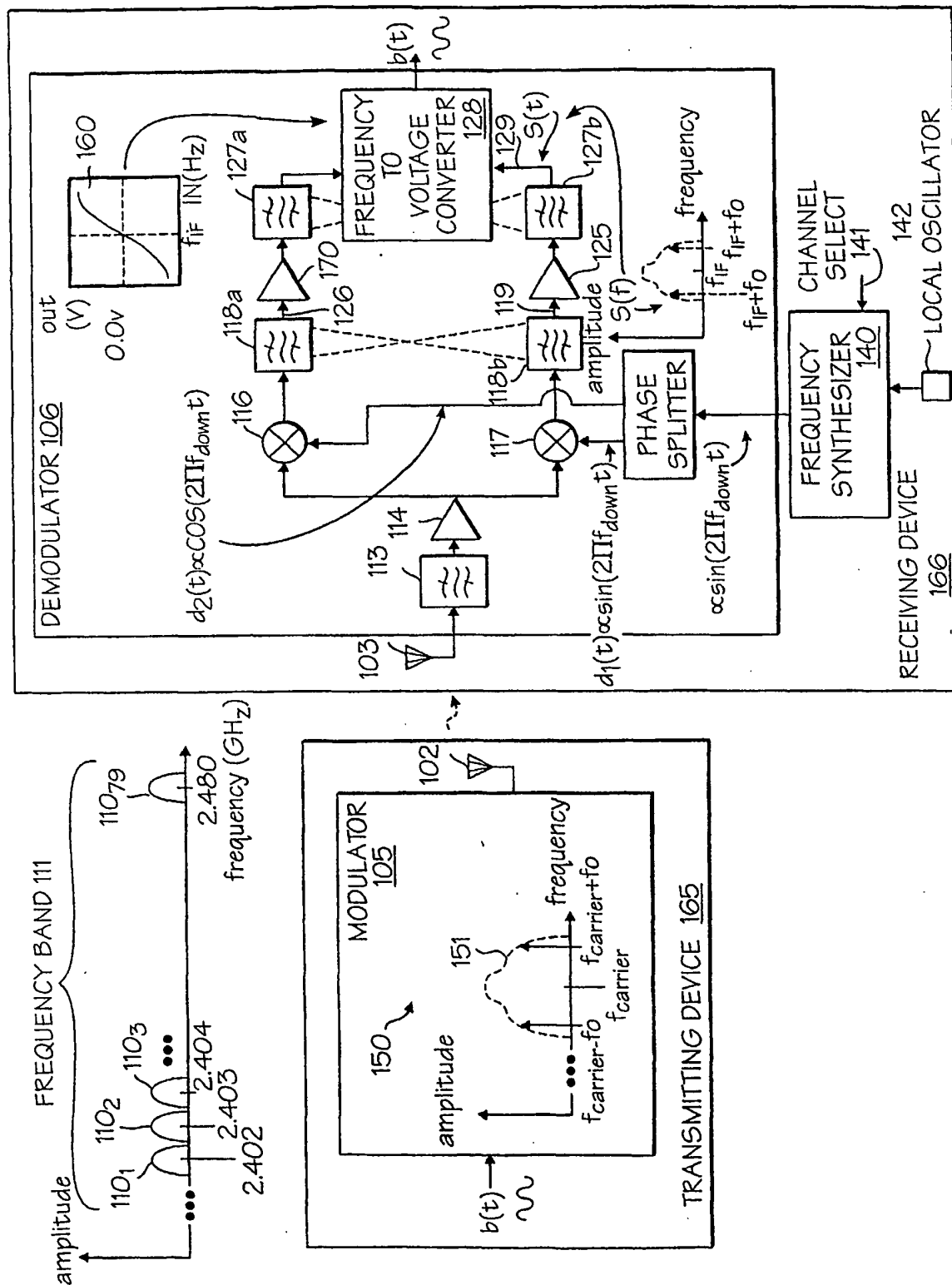


Fig. 1

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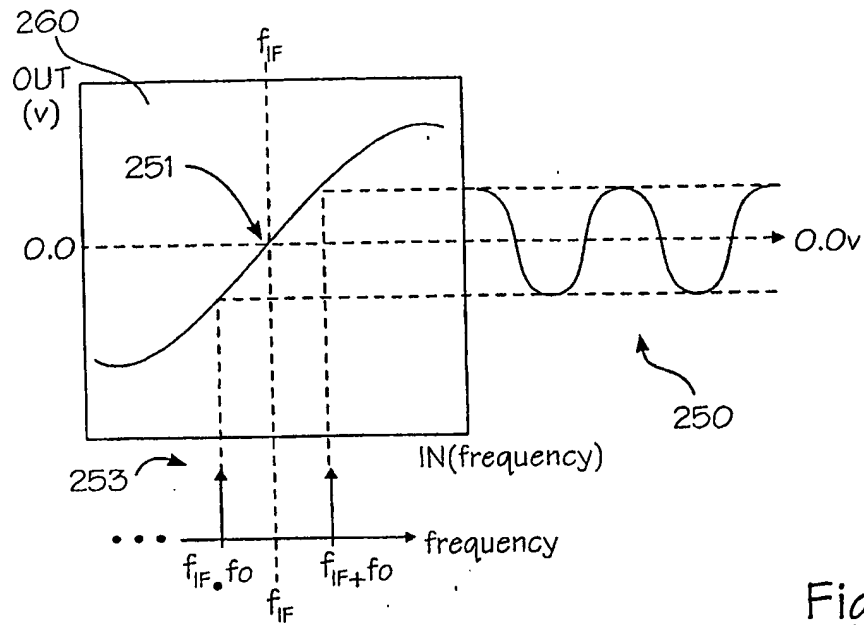


Fig. 2A

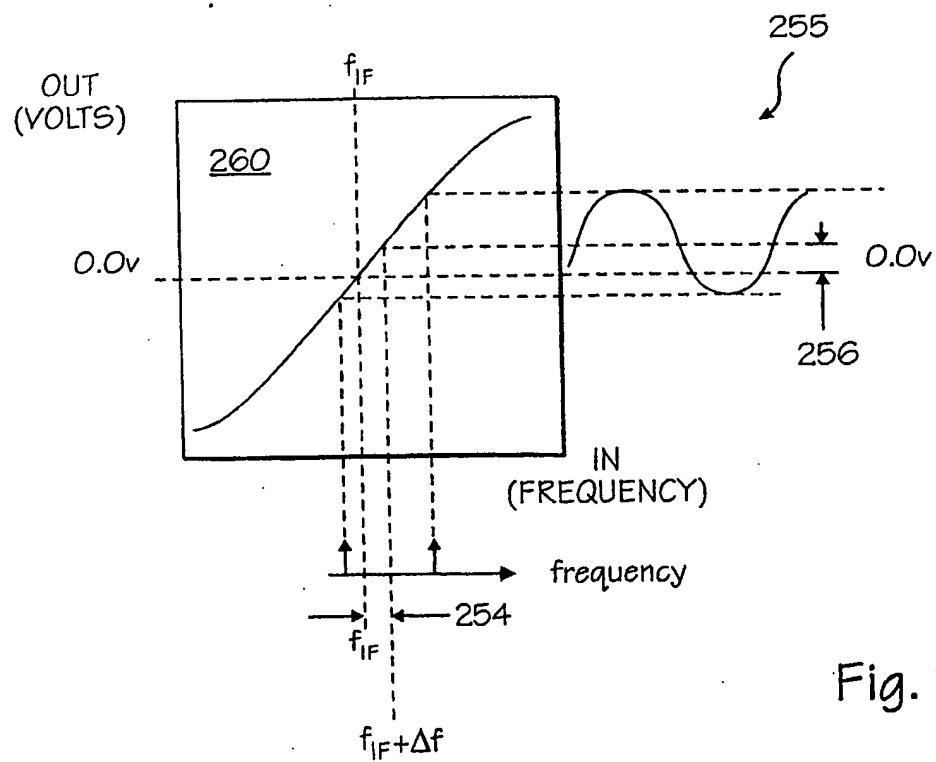


Fig. 2B

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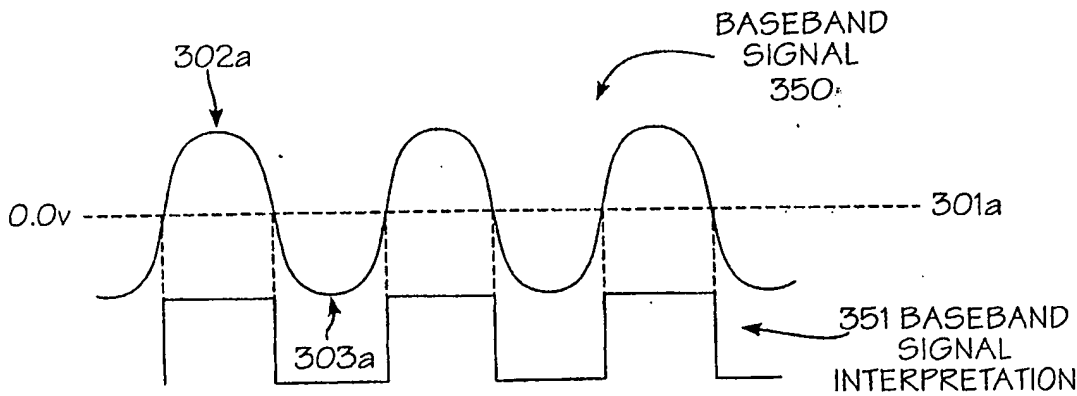


Fig. 3A

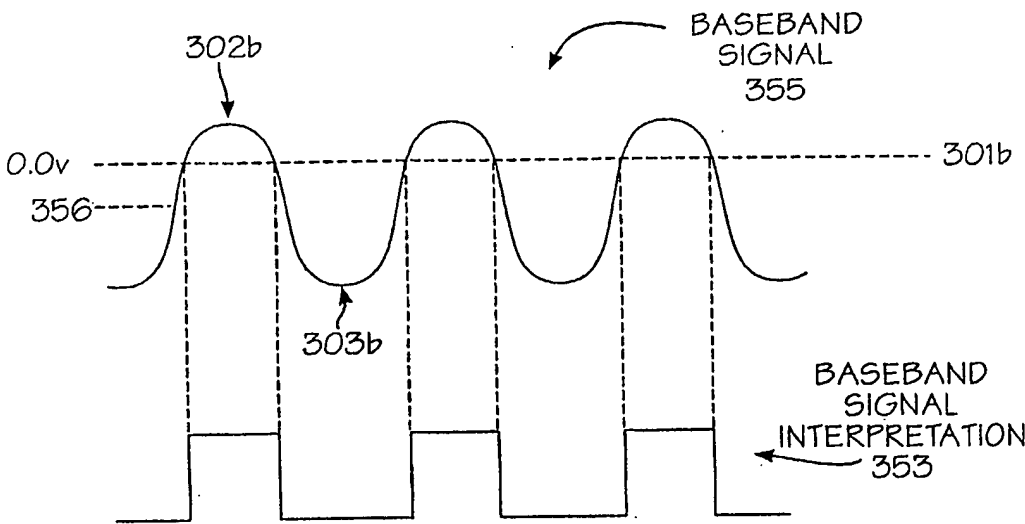


Fig. 3b

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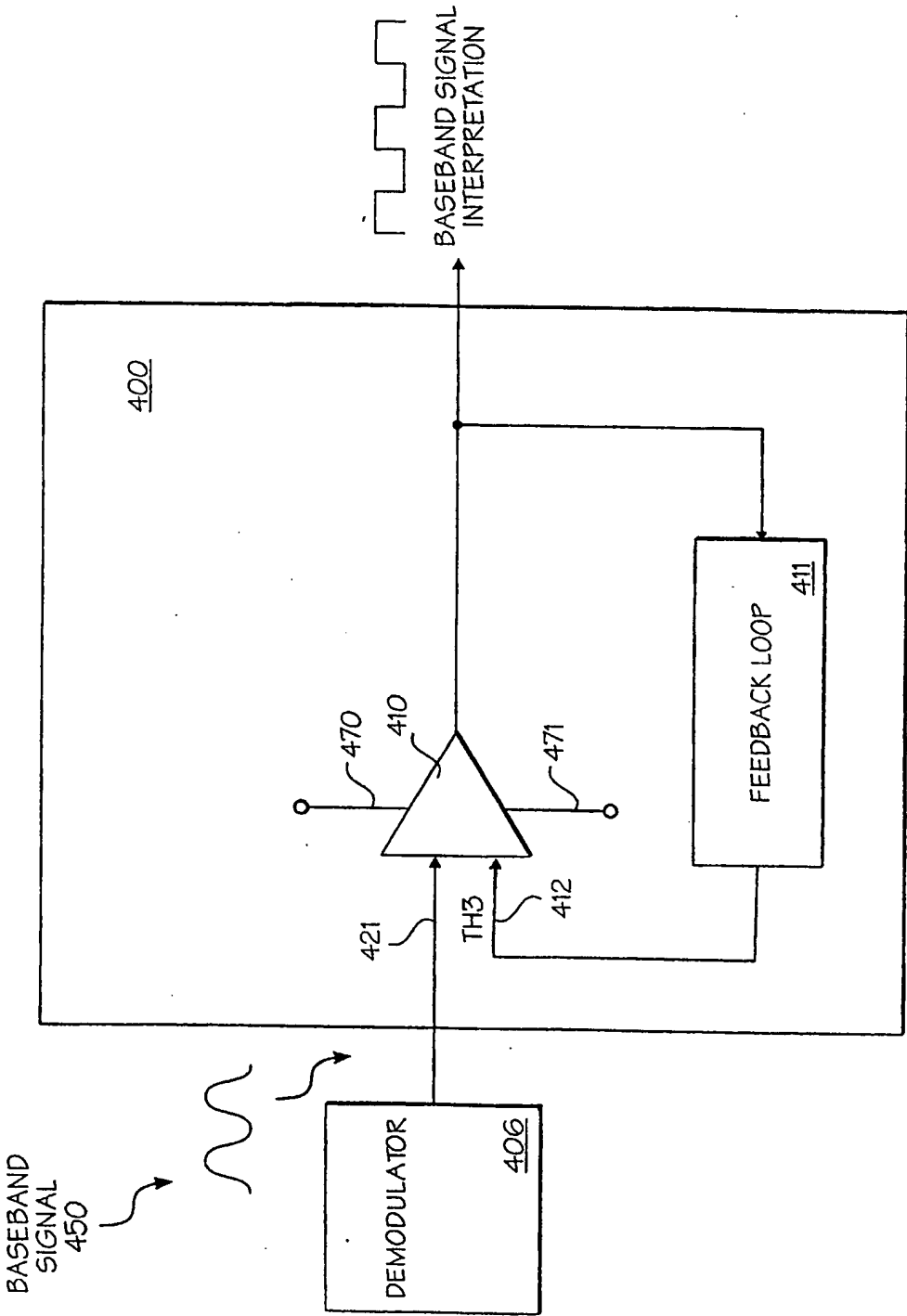


Fig. 4

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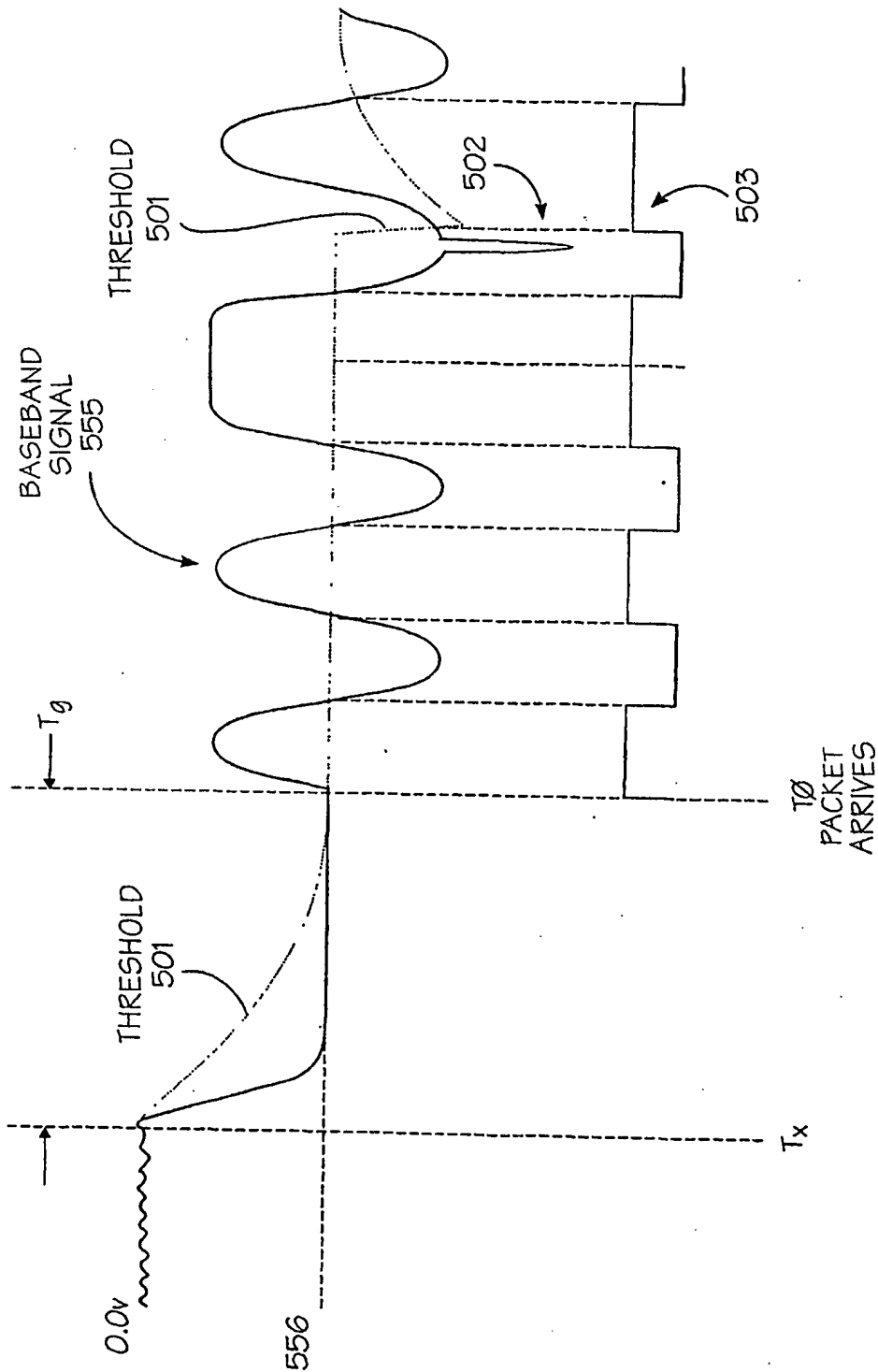


Fig. 5

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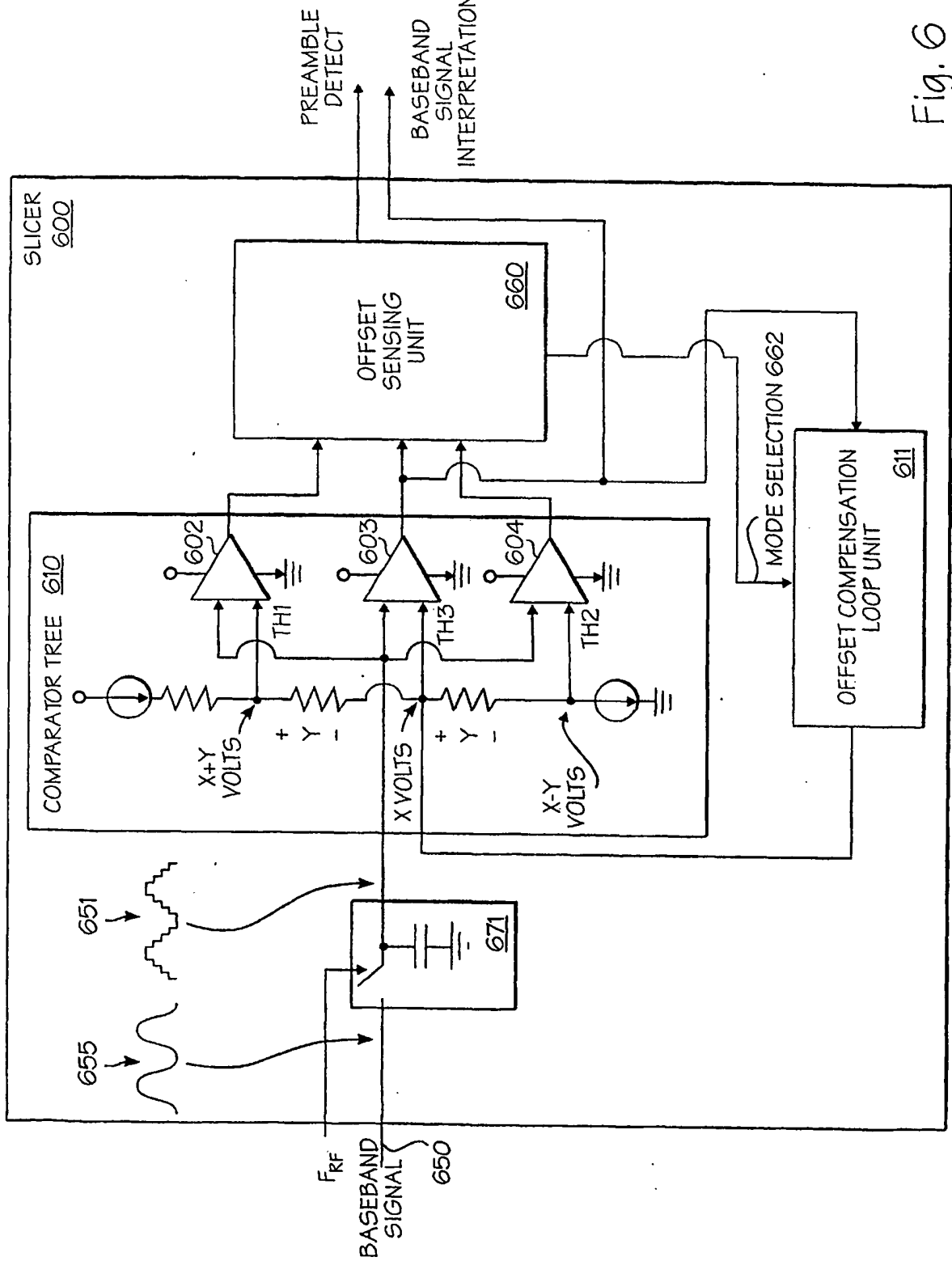


Fig. 6

7/11

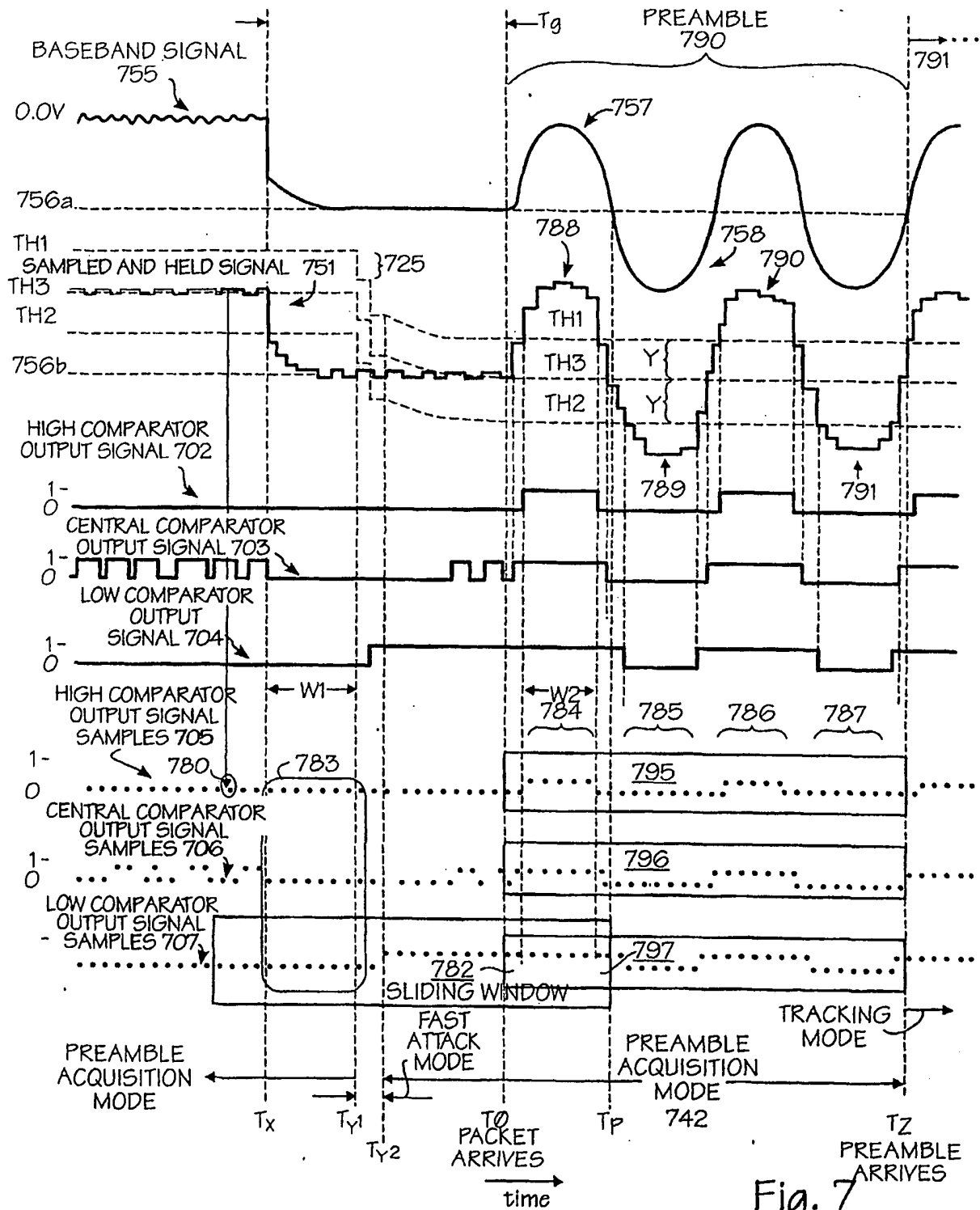


Fig. 7

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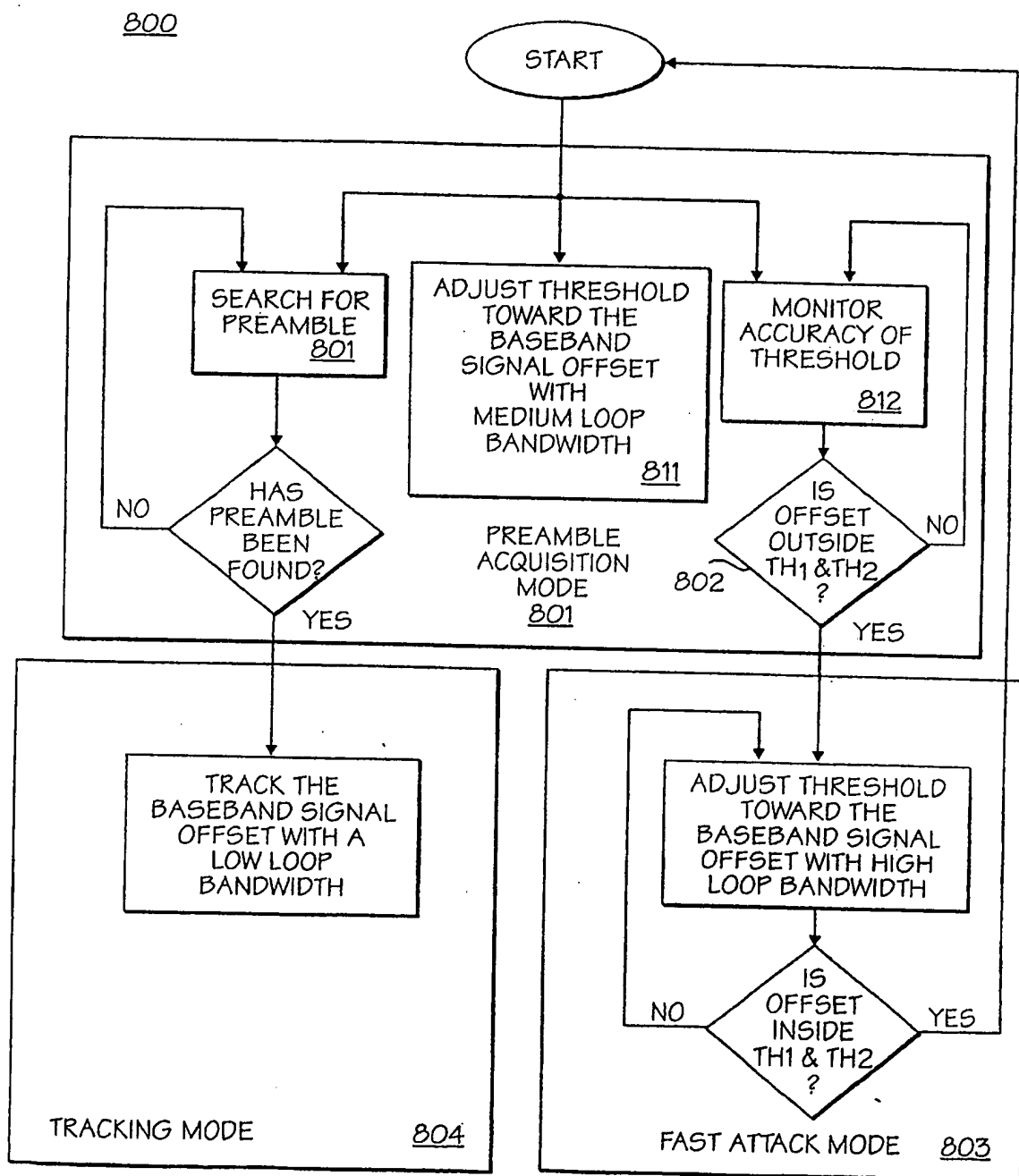


Fig. 8

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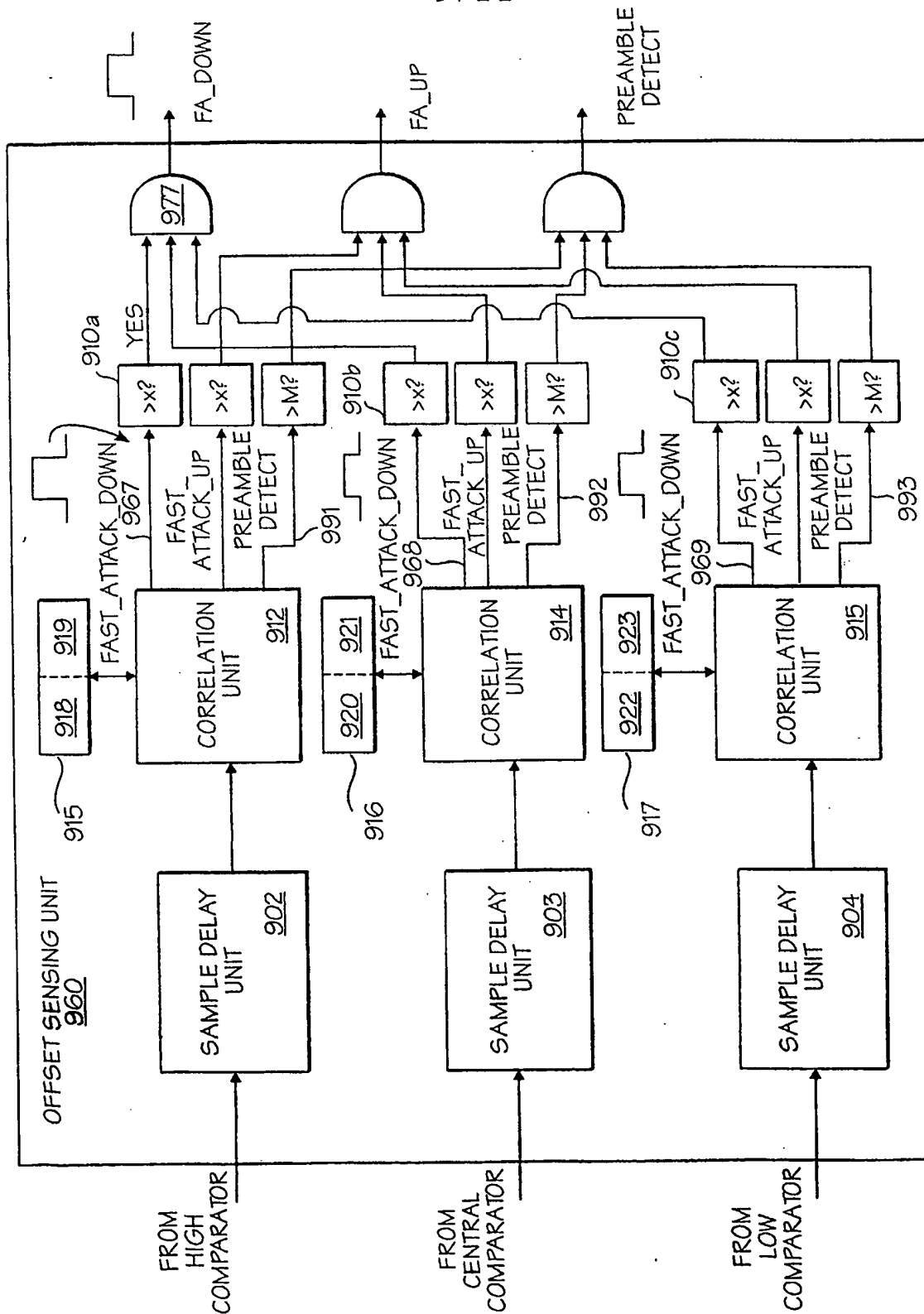


Fig. 9

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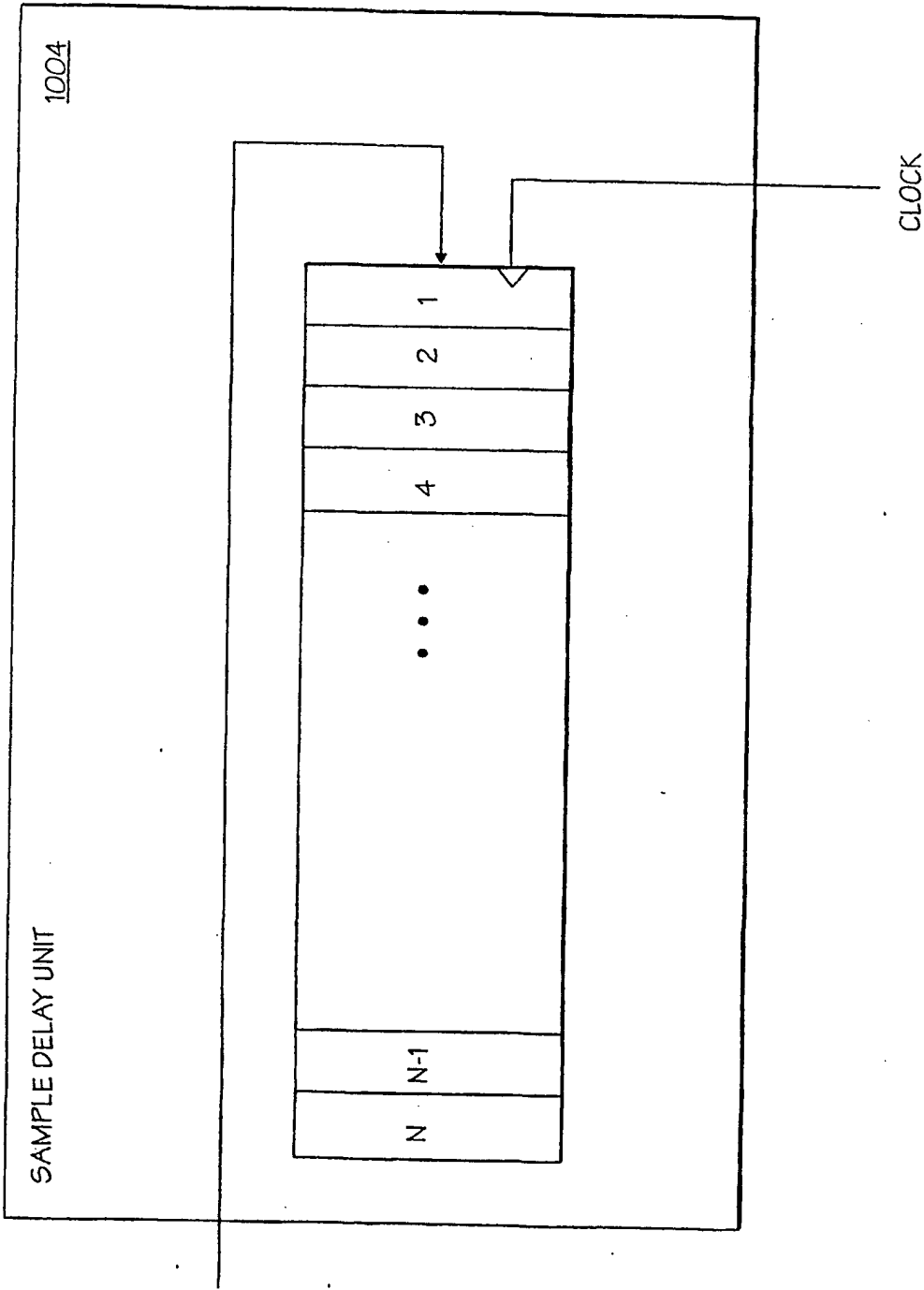


Fig. 10

11/11

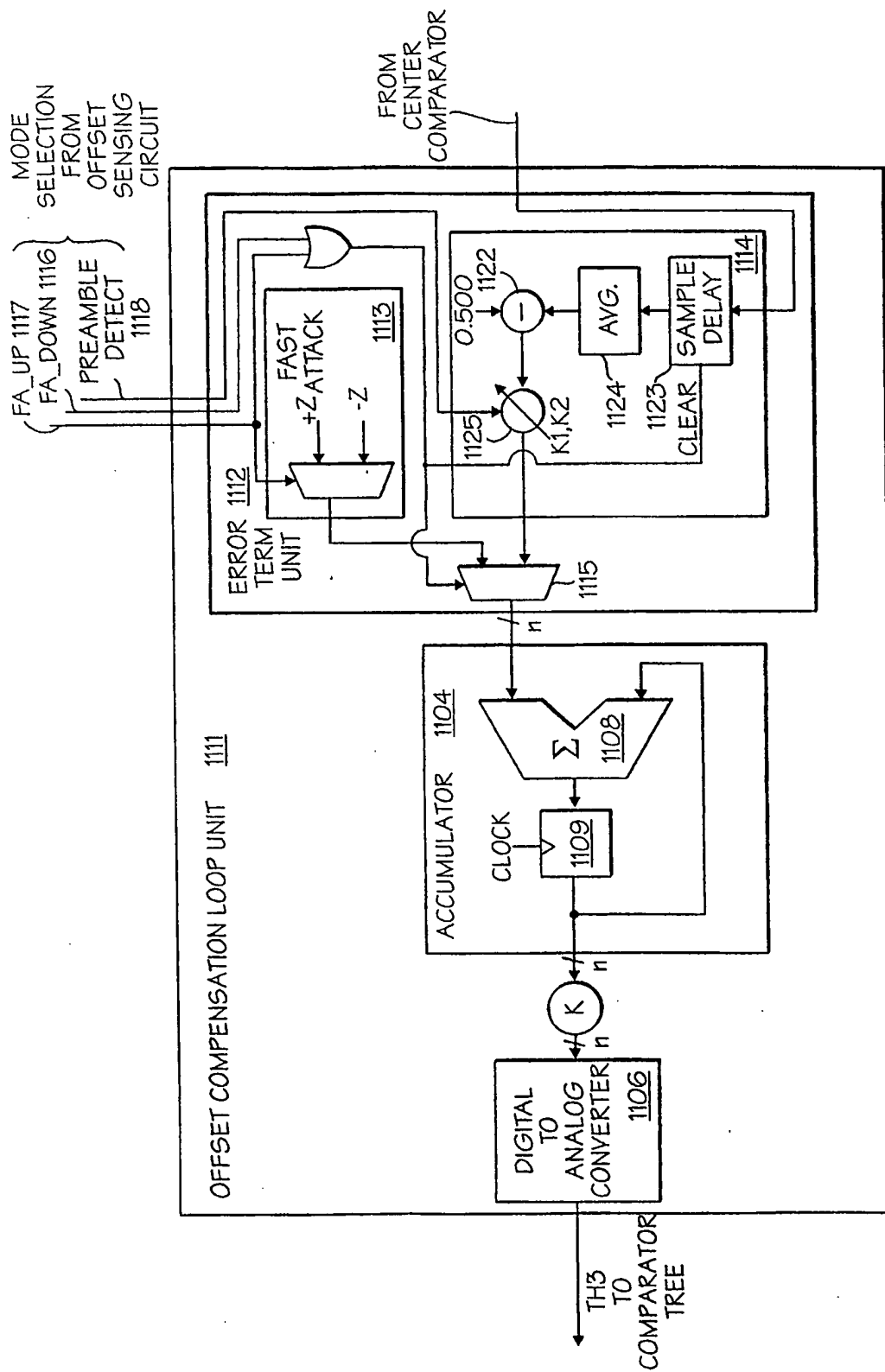


Fig. 11

# INTERNATIONAL SEARCH REPORT

International application No.

PCT/US00/41025

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H04B 17/00

US CL : 455/226.2; 375/272; 327/362; 341/126, 127, 132

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 455/67.1, 226.2, 226.4; 375/245, 272, 316, 317; 327/78, 80, 362; 341/120, 126, 127, 132

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
EAST

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,766,417 A (TAKAYAMA et al) 23 August 1988 (23.08.1988), column 1, line 31 - column 2, line 2.	1-55
A	US 5,262,686 A (KUROSAWA) 16 November 1993 (16.11.1993), column 3, line 50 - column 4, line 39.	1-55
A	US 5,412,687 A (SUTTON et al) 02 May 1995 (02.05.1995), column 6, line 5 - column 8, line 48.	1-55
A	US 5,661,4 A (VALLANCOURT) 26 August 1997 (26.08.1997), column 3, line 5 - column 6, line 6.	1-55

☐ Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T"

later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X"

document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y"

document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"

document member of the same patent family

Date of the actual completion of the international search

22 January 2001

Date of mailing of the international search report

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